A Review of Recent Research on Heat Transfer in Three-Dimensional Integrated Circuits (3-D ICs)

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***Abstract*— Three-dimensional integrated circuits (3-D IC) technology has emerged in the past few decades, driven in part by the techno-economic difficulties of dimensional scaling and the increasing interconnect delay in microelectronics. In a 3-D IC, vertical integration of multiple transistor planes, either through monolithic integration or through bonding of multiple strata, offers reduced interconnect delay and enhanced design flexibility. However, vertical integration in a 3-D IC also results in severe thermal management challenges. Thermal management of a 3-D IC is exacerbated by the multilayer nature of the 3-D IC. Furthermore, new components such as through-silicon vias (TSVs) offer opportunities for novel thermal management. This article presents a critical review of research literature related to heat transfer in 3-D ICs, focusing specifically on thermal modeling, thermal–electrical codesign, and thermal management of a 3-D IC. Key literature from recent years is categorized and summarized. A discussion on the future outlook for research in these areas is presented. It is expected that this review article will be helpful for researchers in academia and industry for understanding the state-of-the-art in various areas related to heat transfer in 3-D ICs.**

***Index Terms*— Codesign, heat transfer, thermal management, three-dimensional integrated circuits (3-D ICs).**

I. Introduction

STARTING with the invention of the transistor [1], continued improvement in the performance of semiconductor microelectronic devices was, for a long time, sustained by process technology innovation that facilitated the microfabrication of progressively smaller transistors and interconnection. This remarkably sustained, exponential reduction in transistor size and increase in speed, as envisaged by Moore's law [2], continued for several decades. However, as transistors become faster and faster, the speed of interconnection between transistors eventually started becoming the rate-limiting step. In addition, for techno-economic reasons, continued scaling down of the transistor size became increasingly cost-prohibitive. This has led, in the past few decades, to "more-than-Moore" innovations for continued improvement in the performance of semiconductor devices that do not rely completely on transistor scale-down [3]. The traditional framework of all transistors built on the same plane has also been challenged, and multiple approaches and advantages of vertically integrated transistor planes have been demonstrated. This approach, often referred to as a Three-Dimensional Integrated Circuit (3-D IC) [4]–[6], has attracted considerable research in several directions. While 3-D IC technology offers several key advantages compared with traditional, planar chips, progress in the adoption of 3-D ICs in commercial products has been steady rather than spectacular. Among the various technical reasons behind this is the significantly increased challenge in thermal management of a 3-D IC. Thermal management challenges in a 3-D IC are more closely coupled with electrical performance and manufacturing than is the case in traditional planar ICs. These coupled phenomena often present critical trade-offs and constraints that must be correctly recognized and accounted for, to maximize the device performance, reliability, and lifetime.

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A. Key Advantages of 3-D IC Architecture

Vertically stacked 3-D ICs offer several advantages over traditional 2-D ICs [5]. Interconnection in a 2-D IC with increasingly complex circuit components can result in the usage of small but densely packed wires over large interconnect distances between functional blocks, leading to substantial rise in signal propagation delay due to increased resistance and capacitance, also known as *RC* time delays [7]. On the other hand, vertical interconnection using through-silicon vias (TSVs) or microconnects [8] in a 3-D IC may lead to smaller wire lengths, and therefore improved interconnection latency. Reduction in interconnect length also reduces the power requirements along with improvement in signal transmission latency and yield of the circuit [8], [9]. For example, a 23% reduction in interconnect power consumption has been reported in a three-tier circuit compared with a single-tier circuit [10]. It has also been shown that the interconnect power and delay can be further reduced by increasing the wire pitch, which reduces the capacitance and resistance per unit length [4].

Referring to traditional 2-D IC designs for devices such as processors, conventional input–output (I/O) pins were used to connect memory and logic blocks generally arranged in the same plane. In contrast, in 3-D ICs, such interconnection is provided by TSVs, which reduces the critical path length and thus enhances the memory bandwidth of 3-D processors [11]. Other key advantages of 3-D IC architecture include reduced package pin count and reduced form factor. The form factor of an IC relates to the size and shape of the circuitry, which

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can be improved substantially due to the usage of the third dimension in a 3-D IC. Such features of 3-D integration may lead to an overall improved chip design process [11].

The 3-D integration also enables significant design flexibility. By separately designing, for example, the memory and logic chips, it may become possible to reuse the same chip for multiple applications. For example, the same memory chip could be integrated with multiple logic chips intended for multiple applications, thereby reducing the time and cost for memory design [8]. The two chips being integrated do not need to belong to the same technology node, and therefore, noncritical features can continue to be manufactured in lower cost manufacturing facilities.

B. Manufacturing and Packaging of 3-D ICs

Two distinct approaches for manufacturing of 3-D ICs have been investigated. The first is a sequential process, in which multiple transistor planes of the 3-D IC are fabricated sequentially on top of the same silicon substrate [12], [13]. This approach is often referred to as monolithic 3-D IC manufacturing. In contrast, the second approach calls for bonding and stacking of multiple die and/or wafers that are first fabricated independent of each other.

The monolithic process uses either seed crystallization or laser recrystallization and produces highly dense interconnection between adjacent layers of the 3-D IC [13], [14]. Even nanoscale monolithic intertier vias have been demonstrated [15]. This approach does not require die alignment or assembly [16]. However, a key challenge in monolithic 3-D IC manufacturing is that of maintaining the quality of lower layers while subsequently fabricating the upper layers primarily due to the high temperature needed in the fabrication process [12]. To overcome this challenge, molecular bonding at relatively lower temperature (around 200 °C) has been used [17]. Other alternatives to avoid undesirable impacts on lower layers include the use of germanium, which has lower crystallization temperature and melting point compared with silicon, the use of pulse anneal for dopant activation, and implementation of high-κ gate dielectric [13]. The use of Ultratech approach, laser spike annealing (LSA), laser annealing [18], and ion cut technology [19] have also been investigated for minimizing thermal damage to the underlying structures.

In contrast, wafer or die-level 3-D integration does not suffer from the key problems in monolithic 3-D integration, due to which it is by far the dominant process choice for 3-D ICs [17], [20]. In this case, individual die/wafers are manufactured separately and then bonded to each other to provide electrical connectivity between die/wafers. 3-D integration has been carried out in face-to-face, face-to-back, and back-to-back configurations, where "face" and "back" refer to the transistor plane and backside of the silicon substrate, respectively [8].

The two key substrate bonding processes used for 3-D integration are metal-to-metal bonding and dielectric bonding. Dielectric bonding, also known as SiO_2 or oxide diffusion bonding, is carried out at room temperature, and thus minimizes thermal coefficient of expansion (TCE) mismatch

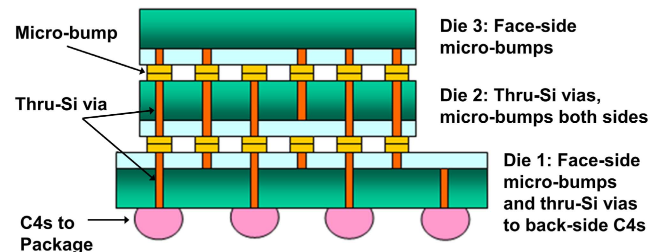

Fig. 1. Schematic of a bonded 3-D chip with three stacked chips (reproduced with permission from [25]).

errors [21]. On the other hand, metallic bonding [20] provides direct electrical connection via TSVs and microbumps, better corrosion resistance, and self-alignment, but is limited in terms of scalability due to TCE mismatch of the interstratum connections [22]. A hybrid bonding that combines metallic and dielectric bonding has also been investigated to combine the advantages of both the approaches [22].

Three distinct approaches have been proposed for 3-D integration—wafer-to-wafer, die-to-wafer, and die-to-die integration [23]. Wafer-to-wafer and die-to-wafer integration approaches have lower yield than die-to-die integration, which offers the Known Good Die (KGD) advantage [24]. However, die-to-die integration may be slower than the other two approaches.

TSVs and die-to-die microbumps are the two key integrating components of a 3-D IC chip stack. While a TSV is primarily used for connecting circuits on two different levels of a 3-D IC, the microbump connects two adjacent chips through bonding processes described above. These components are clearly depicted in Fig. 1, in which the bonding between die 1 and die 2 shows an example of face-to-face configuration, whereas between die 2 and die 3 shows a face-to-back configuration [25]. A TSV is typically manufactured by etching a high-aspect ratio hole through the die and filling it with conductive metal [20]. TSVs along with microbumps on the die/wafer surface enable electrical connectivity between die/wafers. Die thinning through grinding or etching is often carried out to facilitate the TSV manufacturing process [17]. The original wafer is often mounted on a handle wafer prior to thinning to avoid breakage.

Controlling the TSV shape, minimizing the occurrences of voids during metal filling, and preventing metal deposition at TSV edges are some of the key challenges needed to be overcome in TSV processing [26]. Improper wafer alignment is a key reason for TSV failure [27], and approaches such as transparent substrates, wafer backside alignment, through-wafer via holes, infrared alignment, and intersubstrate alignment have been used for wafer alignment [28]. Each TSV displaces transistor space on the silicon, and therefore, a number of interesting optimization problems related to the placement, design, and sizing of TSVs have been investigated [29].

C. Key Thermal Management Challenges in 3-D ICs

Unfortunately, the enhanced packing density in a 3-D IC that leads to reduced interconnect length, reduced power consumption, and other advantages also results in significant thermal management challenges. Higher heat generation in a

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concentrated area fundamentally results in greater temperature rise, which may cause performance reduction and, in an extreme case, physical damage to the circuit. Since one end of a 3-D IC chip stack is usually taken up for electrical interconnection, only one end may be available for thermal dissipation. There may be limited pathways available for heat removal, particularly from chips in the middle of the stack. Supplying coolant fluid into intermediate chips for single-phase or two-phase cooling is also inherently quite challenging. Thermal conduction through TSVs is another heat transfer pathway, for which cooptimization of TSVs is critical. Accurate thermal modeling, thermal–electrical codesign and cooptimization, and effective thermal management approaches for heat dissipation are, therefore, needed to address the thermal challenge in 3-D ICs.

While the cooling of a 3-D IC structure can be carried out using a simple heat sink arrangement for low-power applications, advanced cooling techniques such as single-phase or two-phase liquid cooling may be required for higher heat generation [30]. Regulating the flow rate in liquid cooling can prevent thermal hotspots along with optimization of the overall energy consumption for the cooling system [31]. In general, minimizing pressure drops along the integrated microchannel cooling network is a key challenge [32].

The effective utilization of features specific to 3-D ICs, such as TSVs for heat dissipation, is an important consideration. Thermal-aware floorplanning can manage heat loads by optimum distribution of circuit components and TSVs, to reduce junction temperatures across the IC [33], [34]. Several studies have also been carried out to simultaneously address thermal and electrical design challenges [35]. TSVs have been used as a heat removal mechanism [36], [37]. In addition, hybrid approaches that couple TSVs with microfluidic cooling [38], silicon micropin fin [39], or air gaps [40] have also been reported.

This article presents a critical review of heat transfer and thermal management challenges in a 3-D IC, with particular focus on literature from the past few years since the publication of last major review articles on this topic [30], [41], [42]. Section II discusses key research on modeling approaches for heat transfer in 3-D ICs. Research on the impact of heat transfer on various aspects of 3-D IC design is summarized in Section III. Subsequently, Section IV summarizes the key approaches for heat removal and thermal management for a 3-D IC. Major challenges and future outlook for research in this area are discussed in Section V. The closely coupled nature of manufacturing, electrical design, and thermal management design of a 3-D IC is recognized throughout, with emphasis on the review of articles that address these multidisciplinary challenges. Due to significant overlap between the key focus areas of this article, several articles may be discussed in Sections II–IV.

II. Modeling of Heat Transfer Processes in 3-D IC

Similar to traditional microelectronic chips, the ability to accurately predict temperature distribution in a 3-D IC is critical for accurate 3-D IC design [43]. Furthermore, such a predictive capability is also helpful for run-time performance optimization. Modeling of heat transfer processes in a 3-D IC may be carried out using a variety of techniques. Broadly, these are divided into analytical and numerical computation approaches. Analytical techniques rely on deriving exact solutions of the energy conservation equation that in addition to boundary conditions governs the temperature field. Numerical computations, on the other hand, seek to approximately solve these equations by discretizing the geometry. While analytical techniques are desirable because of exactness and ease of integration with other design tools, it is often difficult to account for complex geometries, temperature-dependent properties, and other complications. On the other hand, numerical techniques, while inherently inexact, may, with appropriate design, offer temperature predictions with acceptable accuracy. In addition to analytical or numerical models that address only the thermal characteristics of the 3-D IC, tools that combine the thermal and electrical design are also critical. This section is organized into subthemes based on thermal modeling applications discussed in the literature. First, heat transfer modeling of the entire 3-D ICs is discussed, followed by analytical and numerical modeling of 3-D IC cooling. Modeling of specific components such as TSVs is discussed next, followed by a discussion of work on interdie thermal contact resistance, further focusing on the modeling of specific thermal properties such as effective thermal resistance or effective thermal conductivity of the 3-D IC.

Extensive literature is available on both analytical and numerical approaches for heat transfer modeling in a 3-D IC. The body of literature is somewhat more limited for analytical approaches. Table I summarizes the key findings and techniques used in the literature on thermal modeling of 3-D ICs. A thermal model of a 3-D IC was developed to compare the thermal performance with an equivalent 2-D IC [44]. It was shown that while the 3-D IC structure has a lower power usage advantage due to shorter interconnects, it may face greater thermal management problems due to insufficient heat removal. It was suggested that heat dissipation components such as TSVs and copper bonds play a more important role than effective thermal resistance to keep the chip temperature within acceptable limits [44]. Another thermal simulation of 3-D ICs, referred to as logi-thermal simulation, was carried out by coupling the logic and thermal parameters [45]. The use of this simulation tool for efficient component placement in 3-D ICs was demonstrated. Furthermore, a transient thermal simulation for 3-D ICs using weighted Laguerre polynomials as basis functions has been proposed [46]. Galerkin's method was used to suppress the effect of time step on simulation stability. Thermal simulations with adaptive time step have also been developed in standard programming languages such as C++ [47], which is important for ultimate integration of thermal prediction tools with other design tools. An adaptive time step simulation was designed to account for both thermal and functional behavior of 3-D ICs. Models for temperature-dependent electromigration (EM) and leakage power have been developed [48]. It has been claimed that power dissipation and thermal distribution across the chip can be efficiently calculated and compared with

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TABLE I
SUMMARY OF TECHNIQUES AND FINDINGS OF RESEARCH ARTICLES ON THERMAL MODELING OF 3-D ICs

Paper	Research Technique	Key Goals/Results
[56]	Fast compact transient thermal modeling: 3D-ICE	Accounts for microfluidic cooling and accurately predicts the thermal distribution with relative error of 3.4%.
[47]	Thermal distributions for 3D IC using adaptive simulation time step approach	Simulation time is reduced by a bigger margin due to the continuously varying time step value depending on past iteration results.
[49]	Temperature gradient aware thermal simulator (3D-TarGA)	Considers the thermal effects due to conduction, convection and radiation along with the leakage power in the 3D IC.
[45]	Logi-thermal simulation for predicting thermal distributions across the 3D IC	To identify the thermal issues and to assist in the component placement algorithms.
[46]	Transient simulation using weighted Laguerre polynomials to predict the thermal behavior of 3D IC	Stability of the method is not dependent on the time steps, due to which it performs better than the conventional methods.
[51]	Thermal distribution for 3D ICs with unequal die sizes using an analytical model	Higher the dissimilarity in die dimensions, higher will be the maximum chip temperature.
[60]	A thermal resistance network for the 3D ICs using heat conduction equation in spherical coordinates	Within 5% of experimental benchmark in the 0.27-2.18 W range of heating power.
[59]	Analytical-numerical modeling for 3D IC thermal behavior	Equivalent thermal resistance for the junction to air pathway
[67]	Equivalent thermal conductivity model for 3D ICs, anisotropic in nature	Considered lateral as well as vertical thermal transmission along the copper wires, TSVs and microbumps, agreed within 7.5% with a finite element code.
[52]	Effect of die thickness on thermal distributions across 3D IC	3D ICs with thinner dies might results into intensified hotspots but comparatively thicker die would work as a heat spreader in lateral directions.
[62]; [63]	Numerical modeling of interdie thermal resistance of the 3D ICs and experimental measurements	Measurement of inter-die thermal contact resistance.

other conventional methods, which do not consider these temperature-dependent factors. Another thermal simulation study named 3-D-TarGA (3-D–temperature gradient-aware–architectural level) thermal analysis was proposed to account for a variety of considerations such as thermal convection, radiation, conductivity, and leakage power [49]. This simulator was claimed to adequately account for the interdependence of thermal and other physical effects in the 3-D IC and was shown to agree well with the experimental benchmarks in terms of maximum IC temperature [49]. Recently, a thermal simulation tool named as Overheat 3-D-IC was developed based on the quasi-3-D thermal design approach [50]. This tool reduces the computational time by reducing the main 3-D heat transfer equation into a group of coupled 2-D equations targeting separate interdie layers. This thermal simulation tool has claimed that it can reduce the computational time to just 10% that of the other commercially available thermal simulators with maximum of 20% relative error in calculation of maximum chip temperature [50].

Thermal distribution across the multidie 3-D IC also depends on the dimensions of subsequent die arranged vertically one over the other. Literature suggests that the differences in lateral sizes of neighboring die [51] or the variations in die thickness [52] may lead to significant change in hotspot locations and intensities. An analytical heat transfer model for thermal distribution in a 3-D IC with unequally sized die [51] has suggested that a 3-D IC with higher dissimilarity in lateral die dimensions results in a higher maximum chip temperature. On the other hand, another work focusing on the impact of the variation in die thickness and interdie bonding materials [52] has claimed that thinner dies lead to a higher probability of large localized temperatures. In contrast, relatively thicker die may act as a heat spreader and facilitate lateral heat transfer. It has been shown that using underfill materials with high thermal conductivity can dramatically improve the thermal performance of 3-D ICs [52]. Additionally in another study, an analytical model for heat transfer in 3-D ICs was developed to optimize the relative arrangement of hotspots to achieve uniform temperature distribution and minimal peak temperature [53]. Thermal conduction analysis has been combined with sequential quadratic programming algorithm to account for the impact of TSVs, heat spreader, and thermal interface material (TIM) [54]. The use of this tool for sensitivity-based optimization for heat transfer in a multilayered 3-D IC has been demonstrated. A thermal model for dissimilar semiconductor chiplets integrated into a single 3-D IC has been proposed [55]. This approach carries out placement of heterogeneous interconnects using customized codes, followed by extraction of thermal properties of the layout material. A fast thermal modeling approach called 3-D-ICE has been proposed for 3-D ICs with intertier microchannel cooling [56]. The stated approach using compact transient thermal model has been claimed to be time-saving and accurate with 3.4% error in peak temperature after validating the same against a commercial computational fluid dynamics (CFD) tool. The 3-D-ICE approach could reduce the simulation time dramatically when compared with a conventional CFD method, due to its capability of parallel operations on multicore architectures [56]. Other analytical thermal models for a multidie stack integrated with interdie microfluidic cooling have also been proposed [57]. Recently, a thermal modeling numerical tool–TIMiTIC–Thermal simulator of Integrated Microchannel cooling for 3-D ICs was used to optimize the profile for power dissipation to reduce the peak temperature by 10 °C [58].

The thermal properties of the 3-D IC structure, such as effective thermal resistance or equivalent thermal conductivity, can help develop accurate thermal models. An analytical model was developed to calculate the thermal resistance of the junction-to-air pathway of a 3-D IC, assuming 1-D heat

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flow [59]. An interesting thermal analysis was carried out for the thermal resistance network in a 3-D IC using the principle of heat conduction in spherical coordinates [60]. A maximum relative error of 5% compared with the experimental results was demonstrated in the 0.27–2.18 W range of heating power. A thermal resistance analysis was carried out for a 3-D IC integrated with TSV interposers and microfluidic cooling embedded in the bottommost TSV interposers in the stack [61]. On the other hand, a thermal model was proposed to determine the interdie thermal resistance in a 3-D IC [62]. Thermal resistance was determined using high-speed temperature measurement on one die while the neighboring die is heated and comparison with a numerical model [62]. A similar technique was used to evaluate the thermal resistance of interconnecting microbumps in a customized 3-D IC chip with and without underfill [63]. Another study involved an experimental benchmarking of a Cu/dielectric wafer-to-wafer bonded 3-D IC, on the basis of which steady-state and transient thermal models were developed [64]. This study confirmed that the use of Cu/dielectric bonding reduced die-to-die thermal resistance. A compact thermal model was developed using finite volume method (FVM) to model the impact of the power distribution network as a heat source [65]. This model determined an equivalent thermal conductivity of a power distribution network, which was then used for temperature calculations. Furthermore, a numerical model was developed to predict the thermal behavior of 3-D ICs based on equivalent, anisotropic thermal conductivity. This model considered several parameters such as TSV dimensions, thickness of linear material, and type of TIM [66]. Similarly, another numerical model for equivalent, anisotropic thermal conductivity of a 3-D IC has been proposed, assuming heat transfer in the vertical and lateral directions in the structure [67]. As shown in Fig. 2, the heat conduction path considered for analysis accounts for copper redistribution wires, TSVs, and microbumps [67].

In light of the several modeling approaches available, as described above, the decision of which approach to adopt for a specific application must consider the degree of accuracy desired and computational resources available. In addition, whether the temperature computation needs to be implemented in real-time is also an important consideration.

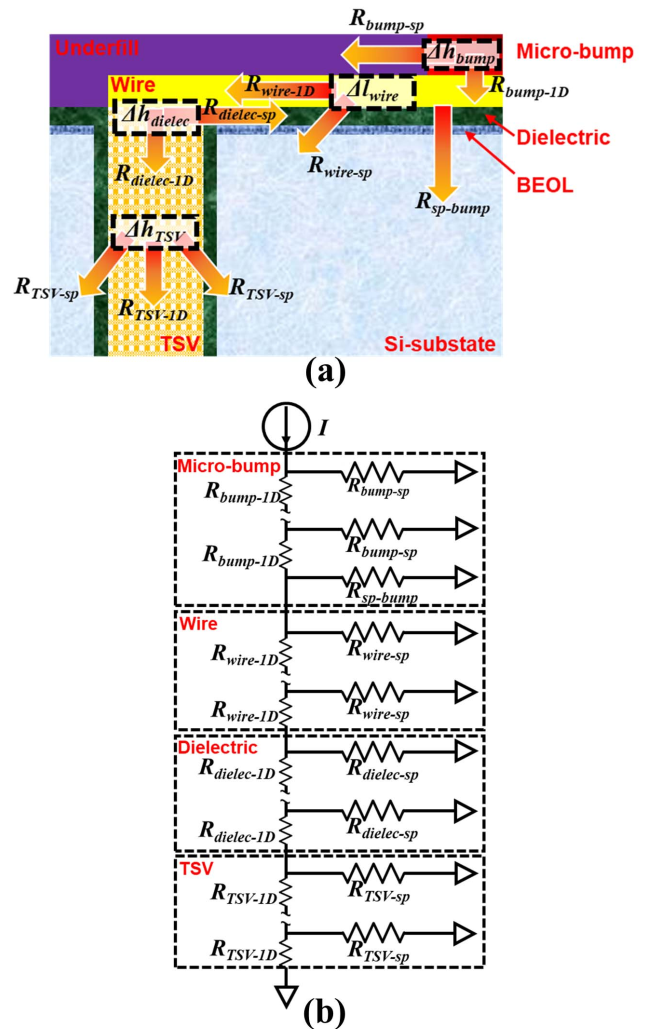

Fig. 2. (a) Basic structures of high thermal conduction path. (b) Compact thermal resistance network of high thermal conduction path (adapted with permission from [67]).

III. Thermal Considerations in 3-D IC Design

A 3-D IC offers key advantages such as lower latency due to reduced wire length and reduced power consumption compared with a convectional 2-D IC. However, higher thermal resistance in the vertical direction due to lower thermal conductivity of dielectric interlayers, interlayer thermal contact resistance, and higher power density in smaller, concentrated areas result in critical thermal challenges, which can severely throttle the chip performance and limit the benefits gained by 3-D integration [68]. These challenges are best addressed in the design stage of 3-D ICs instead of being an afterthought [69], [70]. The key 3-D IC design steps—floorplanning, placement, and routing—must take thermal considerations into account for thermal–electrical codesign and cooptimization [71]. Such kinds of thermal-aware methods are also used to rectify 3-D IC reliability issues based on TSV operations [72]. Accurate prediction of the temperature distribution is particularly important, since a direct temperature measurement is often not possible [33], [73]–[75], [76]. The use of TSVs and thermal through-silicon vias (TTSVs) for promoting heat transfer in the vertical direction has been widely proposed [33]. Efficient placement of TSVs/TTSVs has been carried out to maximize the thermal benefit while also achieving reduced wire length, effective usage of available silicon area, well-managed routing, and overlapping of components [77]. Table II summarizes the key literature in the area of thermal design and thermal–electrical codesign, including the comparison of the outcomes in terms of improvements in key performance parameters with the respective benchmark circuits listed for each article. This section is organized as follows—starting with the thermal-aware placement and floorplanning algorithms for TSVs and other cells in 3-D ICs, followed by a detailed discussion on cooptimization of the thermal and electrical aspects of a 3-D IC, which includes power consumption, signal delay, and heat dissipation

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TABLE II

SUMMARY OF THE IMPROVEMENTS IN PERFORMANCE PARAMETERS IN THE FIELD OF THERMAL DESIGN AND THERMAL–ELECTRICAL CODESIGN OF 3-D ICs FOCUSING ON PLACEMENT OR FLOORPLANNING TECHNIQUES. T_{MAX}, T_{avg}, AND dT/Dx ARE THE PEAK TEMPERATURE, AVERAGE TEMPERATURE, AND TEMPERATURE GRADIENT, RESPECTIVELY. L_{w}, N_{TSV}, AND A_{chip} ARE THE LENGTH OF WIRE, NUMBER OF TSVs, AND CHIP AREA, RESPECTIVELY

Paper	Technique	Comparison	Change (%)					
			T_{MAX}	T_{AVG}	L_W	N_{TSV}	A_{CHIP}	dT/dx
[34]	Iterative thermal force directed approach	A benchmark circuit with placement without thermal forces	-12	-1.3	5			-17
[85]	T3Place: Transformation from 2D to 3D placement	Relaxed conflict net (RCN) graph-based layer assignment	-37		8	6		
[69]	Quadratic uniformity modelling approach	3D placement with thermal considerations	-15	-3	6			
[33]	Pseudo 3D placement considering impact of TSVs	Baseline case	-34		6			
[78]	TSV spread and alignment	Baseline case	-0.3	-2.7	9.3			
	Coupling aware placement	Baseline case	-11	-1.6	9			
[74]	Fast thermal analysis 3D floorplanning with TSV placement	No temperature optimization	-13		1.4	0.1		
[75]	Temperature aware floorplanning without TTSV placement	Baseline case [49]	-46		5	40	7	

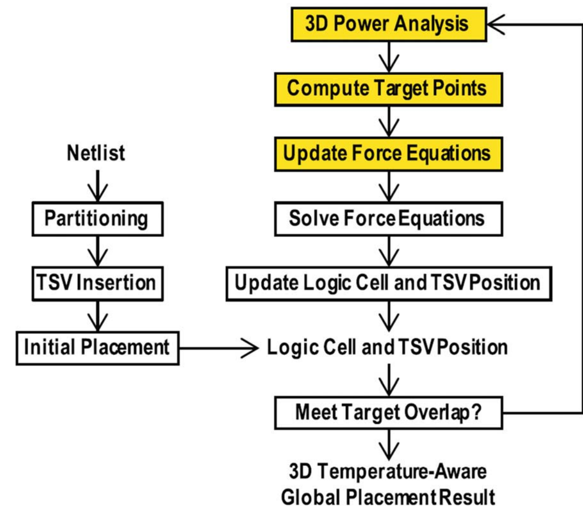

Fig. 3. Design flow for 3-D IC global placement (reproduced with permission from [78]).

requirements for designing the placement strategies. The challenges in the design phase of a microfluidic cooling-based 3-D ICs are also discussed in this section. At the end, the effect of thermal stresses and thermal-stress-aware placement strategies was discussed, which was followed by a discussion on a phenomenon in 3-D ICs called EM.

The introduction of 3-D IC technology has necessitated key changes in the IC design procedure, which now requires determination of wire length and number of TSVs, as well as the floorplanning and placement of the TSVs with respect to other circuit components on the chip. Fig. 3 depicts the general design flow for 3-D IC placement, from TSV insertion all the way to iterative optimization of positioning of TSVs and other components [78]. These tools typically also compute and seek to optimize the thermal impact of the TSVs. A system-level thermal-aware simulation named Pathfinder3D has been developed to generate a 3-D IC floorplan using thermal properties of the components [68]. Pathfinder3D facilitates balancing various design alternatives to discover possible tradeoffs among power, temperature, and performance of the chip without any thorough execution of the generated floorplan based on the available static and dynamic thermal profiles. This simulation uses a physical thermal extractor known as WireX, which produces a thermal netlist from the tentative generated floorplan, using the thermal properties of the components. Furthermore, using AccessNoxim simulator, an Adaptive Thermal Aware Routing (ATAR) algorithm [79] was developed to reduce the maximum chip temperature based on the standard chip manufacturing norms. ATAR uses the weighted sum approach to calculate the propagating cost to prevent livelock and deadlock and achieve uniform thermal distributions with well-managed on-chip traffic experimentally. Several other similar algorithms such as Traffic and Thermal Aware Routing (TTAR) [80], Dynamic Thermal Balance Routing (DTBR) [81], and Thermal Aware Fully Adaptive Routing Algorithm [82] have also been developed. Recently, a modified genetic algorithm was developed to optimize thermal aware 3-D IC multilevel routing toward minimizing temperature rise and minimizing path selection to control the wire length [83]. This algorithm carries out an effective routing process, in which the TSVs are placed in the available white space of the entire 3-D IC, and the final chip package area and routing resources are calculated based on the number of TSVs assigned. Similarly, a thermal-aware placement method was developed based on optimization of maximum temperature and interconnect length [84]. This method has the capability not just to alter the positions of individual components on chip area but also to interchange the different layers of 3-D ICs.

Strategies for thermal-aware placement and floorplanning generally rely on the positioning of cells and TSVs in such a way that thermal hotspots are avoided, and lower thermal gradients are achieved. In one of the studies, an iterative, thermal-force-directed approach was implemented to position the cells away from the higher temperature regions, using finite-element analysis to monitor postiteration transient thermal distributions across the chip [34]. The approach starts with initiating the placement of all cells in a random fashion, and then improving the average cell temperature and wire length iteratively based on the thermal gradient across the chip. Postprocessing is mostly focused on reducing the percent overlap of cells, starting with the z-direction. Validation results based

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on benchmark circuits and testbenches for this thermal-aware placement confirm the improvement in thermal gradient and reduced peak on-chip temperature with a little increase in wire length [34]. Furthermore, an approach with thermal-aware placement of cells in 3-D IC, also known as T3Place [85], has been proposed. This approach transforms the conventional placement strategy for a 2-D IC into a 3-D placement plan and optimizes the maximum chip temperature, wire length, and number of TSVs. Various transformation techniques have been studied. This includes a local stacking transformation technique that results in minimum wire length and a folding-based transformation, which achieves the lowest number of TSVs in the 3-D floorplan. To achieve a reasonable tradeoff between number of TSVs and wire length, the window-based stacking transformation and additional refinement of the 3-D placement using relaxed conflict net (RCN) graph-based layer assignment method has been proposed [85]. A discrete cosine transformation (DCT) approach in conjunction with a quadratic function based on thermal dissipation and cell placement has been used efficiently in a thermal-aware placement uniformity model [69]. In this case, the unified cell distribution and thermal dissipation are updated iteratively. This quadratic uniformity modeling approach is focused on preventing hotspots with a well-balanced thermal-aware 3-D placement that also minimizes the overlapping of cells and reduces the wire length. Lately, a hierarchical floorplanning approach based on TTSV area and positioning optimization was proposed using simulated annealing [86]. This approach has claimed to reduce the peak chip temperature by 6 °C by increasing the wire length by 3.5%. A Q-learning-based thermal-aware routing algorithm was developed for 3-D ICs, which stated to have a better performance than most recent thermal-aware algorithms [87]. Some of the other 3-D floorplanning approaches include one that uses a bio-inspired hybrid thermal management algorithm [88]. This algorithm combines thermal-aware floorplanning with liquid microchannel cooling to reduce hotspots in a densely packed IC [88].

While the general goal of such floorplanning algorithms is to achieve uniform thermal distribution, some hotspots are inevitable, especially since thermal optimization is being carried out in conjunction with optimizing other performance parameters as well. The effect of placement of liquid microchannels near high-temperature regions has been investigated [88]. In this hybrid algorithm, an initial floorplan is designed without considering the thermal conditions of any functional unit and is then optimized based on the thermal condition of each functional unit. The functional unit positions are interchanged with each other iteratively to reduce the on-chip peak temperature. In a recently proposed thermal-aware floorplanning approach without TTSV implementation [75], simulated annealing was used to optimize the maximum chip temperature. This results in an optimized floorplan that optimizes the wire length and cost of manufacturing along with the maximum chip temperature and the number of TSVs. On the other hand, a 3-D floorplanning using fast thermal analysis [74] has also been proposed, which considers TSV allocation to efficiently minimize the on-chip peak temperature and wire length. In this case, thermal estimates are made using bilinear interpolation using presimulated thermal profiles. Considering validation results for this floorplanning approach obtained on benchmarking circuits, when compared with no temperature optimization case, the on-chip peak temperature was shown to reduce by 13% along with very small increases in wire length and number of TSVs by 1.35% and 0.13%, respectively.

Recent research literature has also recognized the nonthermal consequences of the inclusion of TSVs in the 3-D IC design and has proposed approaches for multiphysics analysis and cooptimization. Each TSV occupies a certain silicon area. If the number and size of TSVs are not controlled, then either the die area must increase significantly or the die area available for circuit placement must go down. Thermal-aware TSV coplacement algorithms have considered these aspects in the TSV design process [33]. Considering the benefit of higher thermal conductivity of a TSV, effective distribution of TSVs leads to an improved thermal integrity in 3-D ICs keeping TSV power distribution as an optimal condition. Some of the research in this direction has focused on simulating and optimizing 3-D IC TSV placement considering the impact of TSVs to achieve ideal gate locations with reduced wire length [77]. Additionally, the 3-D IC placement procedure can further be improved by placing high heat-generating components near regions of higher vertical thermal conductivity due to greater TSV density [78]. TTSVs can also be inserted iteratively after analyzing the 3-D thermal map of the IC, so that the peak on-chip temperature will be maintained below baseline levels [89]. Such an approach can reduce the number of TSVs required and interconnecting wire length along with the hotspot temperature.

Since thermal and performance optimization for a 3-D IC are so closely coupled with each other, the need for 3-D IC codesign on the basis of both thermal and electrical performance has been recognized [70], [90]. This codesign involves optimizing the placement strategies for signal-carrying TSVs [91] as well as TTSVs and microfluidic channels which are responsible for heat dissipation [92]. The 3-D IC designer's primary motive is to find a perfect trade-off in routing space allocation of these IC components that will help satisfy both thermal and performance requirements.

Numerous algorithms have been developed for combined analysis of power consumption and heat generation, focusing on parameters such as peak chip temperature, signal delay, and power leakage. A multiobjective algorithm for 3-D processor floorplanning has been proposed based on interlayer partitioning and vertical overlapping [93]. This floorplanning algorithm attempts to avoid the thermal runaway of 3-D IC due to the effects of temperature and power leakage while balancing the thermal–electric performance. Moreover, a partitioning-based analytical placement technique for 3-D ICs was developed to focus on the direct effect of power leakage on chip temperature considering wire length reduction [91]. Thermal placement in this technique maintains an optimal tradeoff between maximum temperature, interlayer TSV quantity, and wire length while keeping interconnection costs as low as possible. It has been reported that for 46% fewer interlayer vias, a 2% reduction in wire length may be obtained. On the

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other hand, by increasing the interlayer vias by 10% and reducing the wire length by 1%, a 46% reduction in maximum temperature can be attained [91]. Also, a 3-D placement and routing technique was established with the objective to optimize electrical crosstalk and amount of power noise. A 3-D global algorithm has also been proposed to consider other requirements such as reduction of peak temperature, whitespace, and interconnection costs [90]. A Steiner routing algorithm has been developed for 3-D IC codesign in two steps—3-D tree construction and refinement. In this case, the refinement process included repositioning of TSVs following an electrical performance limitation, which were originally planned in the 3-D tree construction with thermal optimization of Elmore delay function. This algorithm helps the IC attain an improved thermal–electric performance with low interference and reduced signal noise [94]. Another thermal electrical cooptimization technique combined an electrical delay model and a temperature computation method for 3-D ICs using Green's function method. This approach focused on reducing the interconnect wire length and peak temperature simultaneously. Physical and manufacturing design constraints in floorplanning were considered in this cooptimization process [95]. In another 3-D IC routing method, the thermal–electrical codesign of TSV/TTSV was carried out using an Integrated Multi-Commodity Min-Cost (IMCMC) model to balance signal congestion and temperature within the design space. Using the conditional grid extension method to solve this IMCMC problem, this work reported 8.2% and 30.2% reduction in the wire length and signal delay, respectively, [96]. Furthermore, a combination of power and thermal models was used to analyze and improve the thermal–electrical performance of a 3-D IC. In this case, the power model estimated power consumption using a linear function, while the thermal model used ring-oscillator-based temperature sensors for estimation of heat dissipation of various IC components [97]. A cooptimization approach has been reported, in which interconnect floorplanning was carried out using design of experiments and response surface methodology. This article reported that the microfluidic cooling method is more effective for greater heat removal and reduced signal delay than planning extra TSVs or TTSVs [92].

Microfluidic cooling has been recognized as a prominent approach for heat removal [31], [98] and is discussed in detail in Section IV. Several design challenges associated with microfluidic cooling have also been recognized and are discussed here. These include higher signal delay due to lengthier interconnecting wires and TSVs and challenges associated with wafer thickness [35]. Since leakage power plays a key role in determining overall heat dissipation, and hence temperature rise [99], therefore, the design stage of the microfluidic cooling mechanism must account for latency and power consumption along with the default thermal objectives. A 3-D centric microfluidic heat sink design was discussed in one of the coupled thermoelectric codesign studies, focusing on its impact on TSV capacitance along with thermal resistance and pressure drop interdependencies. It has been reported that as the interlayer thickness increases, the TSV capacitance also goes up, whereas if the TSV aspect ratio

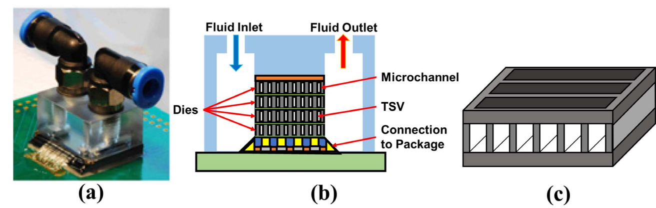

Fig. 4. (a) Prototype. (b) Cross section. (c) Layout of a liquid-cooled 3-D IC (adapted with permission from [31]).

(depth to diameter relation) increases the TSV capacitance gets reduced accordingly [35]. A conjugate analysis of electromagnetism and transient heat transfer has been carried out to simulate an integrated microfluidic cooling based on finite-element method (FEM). This cosimulation efficiency can be improved using schemes such as Finite Element Tearing and Interconnecting (FETI) and FETI-enabled parallel computing combined with adaptive time stepping [100]. For a 3-D FPGA, another case of microfluidic cooling codesign has reported an increase in operative frequency of around 80% and energy efficiency improvement of 124% when compared with a traditional static heat sink. This work has also reported the relationship between microfluidic channel density in single or multiple interlayers with heat removal and electrical performance [99]. In another physical codesign study for a microfluidic-cooled 3-D IC, a hierarchical partitioning-based technique was used to strategically place interlayer micro-fluidically cooled (MFC), circuit gates, and TSVs simultaneously. The advantages of microfluidic cooling over air cooling were highlighted, as it was shown that microfluidic cooling results in 40.2% reduction in chip area [101]. Furthermore, a hierarchical model of online thermal management strategy for a liquid-cooled 3-D IC was proposed. In this work, the thermal profile for a 3-D multiprocessor system on chip (MPSoC) was optimized using dynamic voltage and frequency scaling (DVFS) [102]. Based on experimental validation using benchmarks, thermal variation in less than 10 °C per interlayer and up to 50% energy savings were claimed. In a similar article that also used DVFS-based thermal management, a reduction in energy requirement for cooling mechanism by around 63% and that of the whole 3-D IC by around 21% was reported, without letting the system exceed the set temperature [31]. Fig. 4 describes a microfluidic cooling arrangement of a 3-D IC using a prototype, a cross-sectional view, and a layout of the internal mechanism [31]. Microfluidic pin fin heatsinks embedded in 3-D ICs have been proposed along with a thermo-electric codesign focused on balancing electrical performance and energy efficiency with TSV capacity and cooling capability. This article concluded that the codesign approach improved the performance of 3-D ICs by 123% and 143% based on highest bandwidth and maximum cooling arrangements, respectively, [103].

The generation of thermomechanical stress due to thermal gradient around TSVs leads to serious reliability challenges. A finite-element analysis of copper TSVs has reported that the induced thermal stresses increase as the TSV diameter increases and decreases as the pitch size increases [104]. Due to the thermal gradient and dissimilar thermal expansion

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coefficients of silicon wafer and TSVs, a thermal stress induces a crack driving force to indulge in the silicon, which is dependent on different silicon crystal orientations and TSV depth-to-diameter aspect ratios [105]. Another analysis of thermal stresses in 3-D ICs was carried out to focus on the impact of thermally induced stresses on signal delay, variation circuit timing, and leakage power levels. This analysis has demonstrated the effect of variations in gate placement layouts with respect to the TSVs on signal delay limitations; the path delay can be improved if the device gates are placed in the horizontal planes among TSVs [106]. Furthermore, a thermo-mechanical stress and reliability analysis tool was developed based on linear superposition principle of stress tensors, which is claimed to compute faster than standard finite-element simulation tools in most of the previous studies. This tool suggests that the von Mises stress increases with lower liner thickness and decreases as the TSV pitch increases [107]. A TSV floorplanning strategy to account for and minimize thermomechanical stresses was demonstrated. According to this work, the average thermal stress reduced by 7.6% and 2.2% in block and system level, respectively, [73]. A 3-D IC codesign involving thermal, electrical, and mechanical aspects was proposed, in which a signal delay model was established with the usage of dummy TSVs. It has been reported that if this signal delay model is applied accurately, around 61% reduction in clock skew can be expected [108].

The reliability and performance of IC are negatively affected by the changes in silicon mobility rates due to stresses induced around TSV structures [109], [110]. A keep-out zone is the designated distance of any device from a TSV, so that the device does not get affected due to the induced stress [111], [112]. A thermo-mechanical stress model for copper TSVs in silicon substrate showed that the sidewall roughness of TSVs influences the 3-D IC electrical performance. Leakage current can be reduced with selection of an appropriate etching process to ensure smoother TSV sidewalls [113]. A numerical analysis for thermal stresses induced near TSVs and solder interconnects has established the dependence of TSV and solder joint durability on silicon chip thickness—the higher the chip thickness, the lower the durability of interconnects [114]. This study used general linear model analysis of variance (GLMANOVA) to investigate the effect of each reliability-related factor such as silicon chip thickness, thermomechanical properties of interconnect materials, and TSV aspect ratio. Furthermore, a complement sector model was used to analyze the thermal stresses induced in the 3-D IC TSVs. This analysis concluded that thermal stress is directly proportional to the diameter of TSV [115]. Thermomechanical stresses in through vias in glass substrate have been analyzed [116]. This work showed that the induced thermal stresses increase when the tapered via wall angle increases or the through-glass via diameter and glass substrate thickness decrease. Similarly, a number of finite-element studies of thermal stresses in 3-D ICs are available. These articles characterize different types of stresses and their effects [117]–[120] and investigate the influence of TSV dimensions [121]. On the other hand, a thermal stress analysis based on a knowledge-oriented nonuniform (KONU) refinement strategy with parallel adaptive FEM has been proposed. This method claims to predict TSV-induced thermal stresses with 12.5 times greater speed and 25% greater accuracy compared with a conventional finite-element-based analysis [122]. Additionally, a few attempts have been made to improve the conventional finite-element approach by combining it with artificial neural networks to accurately predict the thermal stresses in 3-D ICs with less computational overheads [123]–[125]. A numerical model for thermo-mechanical stresses induced inside and around the TSV was carried out. A groove structure around the TSV was proposed to effectively release the TSV-induced thermal stress [126]. Recently, a study based on numerical analysis of 3-D IC liquid cooling was carried out which stated the effects of combination of various coolants and different materials of embedded cooling channels on temperature and stress distribution across the chip area were observed [127], [128]. This study highlights the importance of chip fabrication and cooling mechanism design to reduce the localized thermal stress, which may cause cooling system breakdown. Whereas a numerical model focusing on optimizing the thermal stresses and temperature distribution has claimed that around 34% of the reduction in maximum thermal stresses can be achieved by altering the microchannel arrangements and addition of micropin fins [129].

A placement strategy for 3-D IC was proposed based on thermal stress predictions by evaluating different factors such as wire length, electrical performance, induced stresses, and carrier mobility based on keep-out zone dimensions [130]. This placement strategy was shown to have lower circuit latency compared with placement based on optimizing the wire length alone. Another TSV placement technique based on analytical stress migration analysis and von Mises stress estimation was developed and claimed to reduce the von Mises stress by 23% with just 3% extra wire length compared with the conventional placement strategy [131]. In contrast with the extensive literature on modeling and prediction of stresses around a TSV, there is relatively lesser work on experimental measurement. Some of the established methods that have reported for this purpose are micro-Raman spectroscopy [132], precision wafer curvature technique coupled with micro-Raman spectroscopy [133], digital-to-analog test structures [111], X-ray microdiffraction mapping [112], [134], and picosecond ultrasonic method [135].

EM has long been recognized as a key reliability concern in semiconductors [136]. EM, which occurs because atomic diffusion in metal interconnects can, to some extent, be addressed in the design phase [137]. Several articles have been published on EM and its connection with thermal modeling in the design stage for 3-D ICs. A 3-D IC design optimization was carried out on the basis of EM issues due to TSVs, using a compact thermal model and simulated annealing scheme. It was shown that the EM-aware approach can achieve 341% improvement in mean time-to-failure using only 3% extra wire length [138]. Additional work in the EM–thermal-electrical codesign direction has showed that the EM lifetime can be extended by 324% with performance deterioration of just 1%. This study implemented an EM-aware thermal distribution on chip by inserting TTSVs using a quadratic programming-based approach and

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used a linear programming formulation in conjunction to further reduce the wire length [139]. The literature on EM challenges and mitigation in 3-D ICs is somewhat limited.

IV. Thermal Management Approaches for 3-D ICs

Heat dissipation in a 3-D IC is problematic due to the increased density of transistors and interconnection, the use of heterogeneous materials, and the introduction of thermal contact resistances between layers, which may be very large depending on the process technology. These factors may lead to several thermal management concerns such as higher junction temperatures, thermal gradients, and localized hotspots that directly affect IC performance, reliability, and in some cases cause catastrophic failure [102]. Several conventional cooling methods such as air cooling, heat pipes, backside heat exchangers, or thermoelectric coolers are not appropriate for a 3-D IC, in which there is an inherent difficulty in accessing and removing heat from the internal layers within the 3-D IC [140]. Other approaches such as jet impingement cooling and spray cooling also suffer from drawbacks such as the requirement of higher pressures for microdroplet dispersion [141]. Table III summarizes the key outcomes and approaches specified in the research articles on thermal management of 3-D ICs. This section is organized as follows—starting with the concepts of microfluidic cooling, its analytical and numerical modeling, followed by focusing on the micropin fin optimizations in terms of its arrangement and geometry. Furthermore, a discussion about two-phase cooling has been followed by experimental research work in thermal management of 3-D ICs. The importance of thermal TSVs with a motive to mitigate the effects of nonuniform heat dissipation is discussed, ending with the discussion of hybrid approaches in cooling techniques of 3-D ICs.

Microfluidic cooling is the dominant thermal management mechanism that has been investigated for 3-D ICs. Reducing the microchannel cross section generally helps achieve higher heat transfer coefficient and thus higher thermal performance [140], [141], although this may come at the cost of increased pumping requirement. Early work in the use of liquid cooling of integrated circuits used a compact water-cooled integrated heat sink on the backside of the substrate [142]. This study used deionized water at 23 °C and 214 kPa through microchannels etched in silicon, while a thin-film resistor was used as a simulated heat source. A highest substrate temperature of 71 °C and power density of up to 790 W/cm^2 was achieved. It was shown that increasing the coolant flow rate can effectively reduce the thermal resistance. A maximum thermal resistance of 0.09 °C/W per cm^2 was reported. Large pressure gradients along the coolant flow path, sudden drop of thermal performance due to critical heat flux (CHF) limitation, or the discrete flow behavior in terms of coolant phase transformation along the flow have been identified as key challenges [30], [141]. A number of approaches such as optimization of microchannel design [143]–[145], use of micropin fins [146], [147], and achieving controlled flow boiling [148], [149] have been identified.

The design of microfluidic cooling for 3-D IC is fundamentally different from the traditional cooling for 2-D ICs. The interactions between electrical, thermal, and physical design elements become more important than ever, leading to the need for effective, multidisciplinary design tools. The interdependence between microfluid cooling and the electrical, thermal, and physical features of a 3-D IC has been studied [98]. It has been shown that microfluidic cooling cooptimized with floorplanning of a 3-D CPU can improve performance by 130% compared with an air-cooled CPU. Moreover, transient thermal models for liquid cooled 3-D ICs have been developed, with emphasis on improving computational efficiency [150]. One particularly interesting insight from such articles is that for thermal simulations of microfluidic cooling of 3-D ICs, replacement of the fluid region with a simpler convective boundary condition may result in significant improvement in simulation time while keeping the error within acceptable limits [151]. Key limitations of this approach include the ability to model only a straight microchannel in a single interlayer and the inability to account

TABLE III
Summary of Approaches and Outcomes of Research Articles on Thermal Management Techniques in 3-D ICs

Paper	Approach	Outcome
[98]	Co-optimization of floorplanning based on electrical, thermal and physical features of 3D IC with microfluidic cooling.	Performance improvement by 130% compared to an air-cooled CPU.
[158]	Optimization using fast thermal model for liquid cooling networks with flexible topology	Around 84% energy savings in pumping power or reduction in thermal gradient by 38%.
[160]	Independent interlayer microfluidic cooling	Reduction in the junction temperature of a memory-on processor 3D IC by around 25 °C compared to air cooling.
[39]	Microfluidic cooling with combination of TSVs and micro-pin fin heatsinks	Reduction in peak temperature of the circuit by 33% when compared to conventional air-cooled heat sink.
[194]	Microfluidic cooling in conjunction with thermal through silicon vias (TTSVs)	Around 56% energy savings in pump power.
[156]	Non-uniform microchannel distribution	Up to 80% energy savings in cooling system.
[204]	Microfluidic cooling with microgaps and variable pin fin clustering	Maintaining maximum temperature below 65 °C with deionized water at inlet temperature of 21.3 °C.
[147]	Effect of clustering of micro-pin fin in microfluidic cooling	8 °C peak temperature reduction at the expense of 148% increase in pumping power.
[146]	Variable fin density of offset strip fins and variable spacing ribs in microfluidic cooling	30 °C temperature difference and 34 kPa pressure loss for optimum arrangement of variable fin density.
[143]	Microchannel patterning and pruning in microfluidic cooling	Energy savings in the range of 11-61% in terms of cooling system.
[181]	Using vacuum gaps and chip-to-chip communication for thermal isolation	Enables the DRAM to operate at a temperature of 47 °C lower than that of the conventional system.
[202]	Thermal isolation using air gaps in microfluidic cooling	39 °C reduction in peak temperature by compared to conventional design with underfill and microbumps.

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for convective heat transfer coefficient that may vary along the flow path. Other compact thermal modeling techniques have also been developed specifically for straight microchannels with laminar flow of coolant, to be used for logi-thermal simulation framework [152]. This presented model based on a Successive Node Reduction (SUNRED) algorithm has been validated against a CFD software and realistic measurements carried out with different coolant flowrates applied to a microfluidically cooled 3-D IC, with errors around 5%.

A large body of literature exists on the design and optimization of a 3-D IC microfluidic cooling in the form of analytical or numerical modeling. Such models are often validated on experimental test benches prior to fabrication [153]. For example, in one particular 3-D IC design, copper TSVs integrated with microchannels at an areal density of 2500/cm^2 were shown to result in a thermal resistance of 0.24 °C/W, a significant improvement over a traditional air-cooled chip [32]. A thermal model considering the thermal wake effect combined with channel merging techniques was reported, which resulted in significant improvement in computational time within 5% of error when compared with a well-established tool based on FVM [154]. Thermal wake is an effect due to drastic variation in fluid temperatures from solid surface to fully developed boundary layer region, which must be taken into consideration for a fast and accurate model to design an efficient microfluidic cooling mechanism for the 3-D ICs. A thermal management technique focused specifically on hotspot management has been proposed, which used microchannels interconnected with through-silicon fluidic vias (TSFVs) [153], [155]. This study reported an application of this approach to be used in handheld portable devices, since it can be used for mitigating the effect of hotspot but not necessarily for reducing the global temperature of a 3-D IC. In contrast, a thermal model has been developed for nonuniform placement of microchannels to mitigate the impact of localized heat generation [156], [157]. This approach accounted for microchannel placement limitations due to thermal imbalance and TSV complex distribution and concluded that there may be up to 80% power savings in cooling costs when optimally placed compared with uniform placement over the entire chip area. Another fast thermal model has shown around 84% savings in pumping power or reduction in thermal gradient by 38% when compared with straight microchannels [158]. In addition to such articles that focus on thermal aspects of microfluidic cooling in a 3-D IC, analysis of the effect of liquid cooling on electrical parameters of TSVs has also been presented [159]. Based on studies on a micropin fin arrangement with distilled water as a coolant, this work recommended that TSVs must be appropriately shielded from the surrounding coolant. Fig. 5 shows a schematic and SEM of a micropin-fin heat sink with coaxial-like TSV configuration, in which a signal TSV is surrounded by multiple ground TSVs connected by an annular metal pad [159].

A number of mechanisms motivated by traditional heat exchanger design have been proposed for microfluidic-based cooling of 3-D ICs. These include varying the arrangement of microchannels with respect to each other, modifying geometry along the coolant flow path and adding pin fins as flow restrictions to increase the contact surface area. Independent liquid cooling for each tier in a 3-D IC has been investigated [160]. By addressing the power level in each tier separately, this approach was shown to reduce the junction temperature of a memory-on processor 3-D IC by around 25 °C along with a reduction in junction temperature difference among neighboring tiers by around 5 °C compared with air cooling. In another thermal simulation optimization approach, channel patterning was used to diminish hotspot effects and channel pruning to reduce temperature gradient across the 3-D IC [143]. When compared with the standard benchmark, 11%–61% reduction in energy costs and 49%–59% reduction in pumping pressure were reported. Closed-form correlations for converging–diverging microchannels have been used for design microchannel cooling for 3-D ICs [144]. In another study, a thermal simulator based on a clustering algorithm was developed to model a thermal management approach where the microchannels are arranged in the form of clusters [145]. Based on this thermal model, significant reduction in thermal variations across the IC and peak temperature was reported. Microstrip fins or ribs integrated in microchannels with variable densities have been shown to help reduce temperature variations when compared with a continuous pin fin arrangement. A numerical study has studied the impact of density of offset strip fins and variable spacing ribs and reported a temperature difference of around 30 °C and 34 kPa of pressure losses as the highest recorded performance of their variable fin density arrangement [146]. A compact thermal model has been presented for optimization of microgaps and dimensional analysis of micropin fins [161]. This study reported higher convective heat transfer and thus better thermal performance with smaller pin fins in the case of nonuniform heat generation, which also reduces leakage current. In a related another numerical study of a thermal management technique for a 3-D IC with microfluidic cooling, the effect of clustering the micropin fins was studied [147]. Even though a decrease in the peak temperature of around 8 °C was observed, it was accompanied by an increase in pumping power of around 148%, since the pin fin clustering leads to higher flow resistance. Hierarchical partitioning-based thermal strategy for micropin fins embedded in microfluidic cooling of 3-D IC has been studied. This work highlights the importance of considering TSV and metal gate placements to cooptimize the interconnect length and temperature variation along the 3-D IC [162]. This analysis resulted

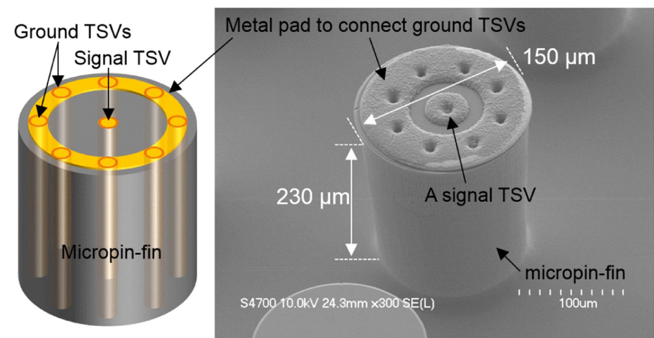

Fig. 5. Schematic and SEM image of micropin fin with coaxial TSVs (reproduced with permission from [159]).

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in around 75% reduction in interstrata temperature difference, around 25% reduction of maximum junction temperature at the expense of 13% extra cost of interconnect length. A recent study has shown that the orientation and location of fins plays a major role in terms of heat dissipating capabilities of the thermal management system [163]. This study concludes that the fins positioned near and oriented toward the hotspots make it more efficient. On the other hand, an annular cavity micropin fin arrangement was tested numerically and experimentally [164]. This system has proven that it reduces the maximum chip temperature by 9 °C and thermal resistance by 34.5%, when compared with standard fully solid fins.

Two-phase cooling involving boiling of the coolant flow has been widely investigated for 3-D IC cooling [42]. In general, two-phase cooling can be a promising alternative to single-phase liquid cooling due to the high heat dissipation capabilities of evaporative mechanism [30], despite several known challenges. Considering the limiting factor of CHF of the coolant, if the IC-produced heat flux surpasses the CHF of coolant, then the cooling mechanism might come across the possibility of dry-out due to the vapor blanket formed on the hot surface [149]. Therefore, to achieve the best performance out of a two-phase cooling system and to avoid damage due to sudden rise in localized hotspots, a coolant selection with CHF higher than the designed IC heat flux is recommended. A thermal model has been developed to theoretically predict the performance of flow boiling along microfluidic straight channels for 3-D IC cooling [148]. This model predicts spatial temperatures in logic and memory regions based on their respective power dissipation levels, claiming peak temperature to be around 85 °C and heat dissipation capability up to 135 W/cm^2. Furthermore, thermal analysis of two-phase cooling in microchannels with nonuniform heat generation has been presented. Performance comparison with single-phase cooling approach has been carried out based on their effects on TSV dimensions and interconnect densities [165]. Analysis of refrigerants such as R123 and R245ca for two-phase cooling has been carried out, showing better performance than single-phase coolants operational around 300 W/cm^2, in terms of reliability and suppressing the localized hotspots. A CFD analysis focused on comparison of single-phase cooling and two-phase cooling with water and R134a, respectively, has been reported [149]. This study has concluded that the two-phase cooling will be superior to single-phase cooling only in the scenario when applied heat generation is below 12 kW/m^2, keeping mass flow rate identical in both cases. A thermal model was proposed for an evaporative interlayer cooling system for a 3-D IC, focusing on effect of hotspot placement on overall thermal management [166]. This finite-difference model showed the importance of an interlayer heat spreader for successful balance between thermal loads generated and heat dissipation in the system. Furthermore, a compact thermal simulation tool—simulation of two-phase energy and mass balance (STEAM)—was developed and validated against experimental data recorded in past studies; this iterative simulation claims that the relative error for temperature prediction for hotspots and spatial heat fluxes was around 7% and 10%, respectively, [167]. A conjugate model was developed to determine fluid flow and heat transfer parameters for the two-phase microchannel cooling system, based on a thermal test vehicle [168]. Fig. 6 depicts a general schematic of the test vehicle connected to a test system [168]. From the experimental validation, it was concluded that the variations for thermal and fluid pressure predictions were well within an accepted range of values. A similar numerical study was carried out to observe the effect of flow boiling on microchannel pin fins with variable density, using a dielectric refrigerant hydrofluoroether (HFE)-7200 as a coolant [169]. Coupled multiphysics models comprising phase change and volume of fluid models have been developed; to study bubble path variations, changes in vapor quality and other thermal, and fluid flow aspects due to nonuniform heat flux distribution [170] and diverging microchannels [171]. Diverging microchannels were proven to perform well under instable flow boiling conditions when compared with that of straight microchannels [171]. Furthermore, it was also reported that compared with rectangular microchannels, zigzag microchannels help suppress flow instability and enhance heat transfer in a two-phase microfluidic cooling system [172]. Recently, an attempt of using a two-phase cooling system with hydrofluoroolefin (HFO) 1234ze nanofluid was carried out to maintain the maximum temperature below the designed threshold –70 °C; this study was also validated in simulated environments along with real system comparisons [173].

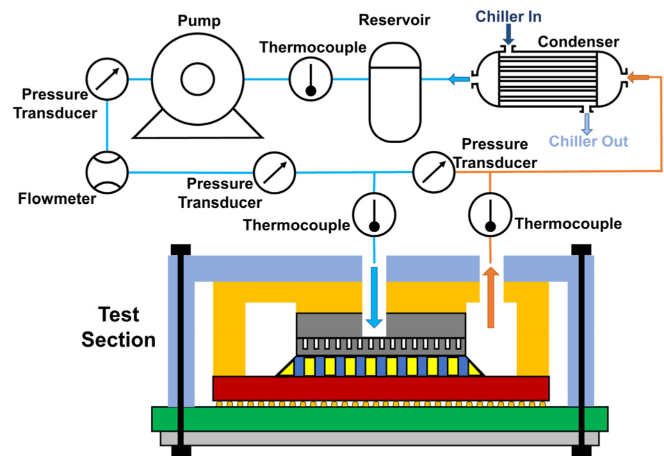

Fig. 6. Schematic of a test vehicle connected to a test system (adapted with permission from [168]).

In addition, several articles have carried out experimental investigation of microfluidic cooling of 3-D ICs, focusing on experimental parameters such as coolant flow rate, thermal resistance, and achievable temperatures. A similar experimental study for single-phase microfluidic cooling used water at 22 °C in one case and a fluorinated fluid capable of operating at subambient temperatures ranging from –40 °C to 20 °C in another case, resulting in cooling capabilities of 500 and 270 W/cm^2, respectively, [174]. In this work, an improvement in the thermal resistance from 15.9 °C-mm^2/W to 12 °C-mm^2/W for water-based microfluidic cooling was reported with the use of an in solder-based TIM instead of a silver epoxy layer. Furthermore, experimental estimation of thermal performance of microfluidic

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cooling in 3-D IC was carried out in comparison with an air-cooled system. The two competing approaches were tested against different combinations of arrangements and power levels [175]. A significantly lower thermal resistance for microfluidic cooling was reported compared with air cooling of the 3-D IC (8 °C-mm^2/W versus 55 °C-mm^2/W). Moreover, to mitigate the complexities of etching microchannels onto the backside of a thin silicon substrate, an alternative approach was suggested in which backside cooling is combined with a microchannel integrated add-on die considering the localized hotspots [176]. Direct contact of coolant with the chip backside resulted in a viable alternative to complicated silicon-etched microchannels. Thermal resistance of 28 °C-mm^2/W with a temperature difference of 55 °C for 20-W power dissipation was reported. Additional experimental study was proposed which focused on the thermal performance of silicon integrated micropin fin arrays and its comparison with that of the conventional microchannels [177]. The convective heat transfer coefficient was measured to be 18.2 kW/m^{2}K and validated with numerical analysis carried out in ANSYS Fluent. An experimental study was carried out with a microfluidic cooling system having arrays of micropin fins, which suggested to operate the flow conditions keeping Reynolds number below 300 after validating the experimental results with standard correlations [178].

In addition to microfluidic liquid cooling, the use of TTSVs has also been widely investigated. In contrast with microfluidic cooling, TTSVs offer passive thermal management, even though there may still be significant space constraints associated with TTSVs [179], [180]. In addition, isolation of critical IC components from high heat generation in the surrounding [181], [182] and use of high thermal conductivity materials for effective heat dissipation [183], [184] have also been reported. TTSVs are also considered as an effective way of heat dissipation by improving the heat transfer path from hotspots to the heat sink with implementation of techniques such as placing TTSVs in an efficient arrangement using a thermal simulation [179] and using redistribution layer along with TTSVs in the 3-D IC silicon oxide interlayers [180].

It has been reported that the use of copper as the TSV material improved the vertical heat transfer across stacked chips compared with the conventional TSVs [36]. In this study, an empirical equivalent relationship for the heat transfer effect of TSVs in 3-D ICs has been proposed. In a related work, equivalent models of 3-D ICs with TSV-integrated interposer were developed. Specifically, equivalent anisotropic thermal conductivity value was determined for copper-TSV interposer with SiO_2 lining [185]. Moreover, a switching algorithm for the signals transmitted via TSV clusters has been developed with the goal of distributing heat generation uniformly over the chip area and suppress hotspots [186]. Experimental validation of a thermal finite-element model was carried out on a 3-D IC test chip featuring Cu–Cu bonds and TSVs [187].

The effects of TSV placement and various associated trade-offs have also been widely researched. Much of the literature in this direction has already been covered in Section III. In the specific context of thermal dissipation through TSVs, thermally aware TSV placement and the corresponding logic

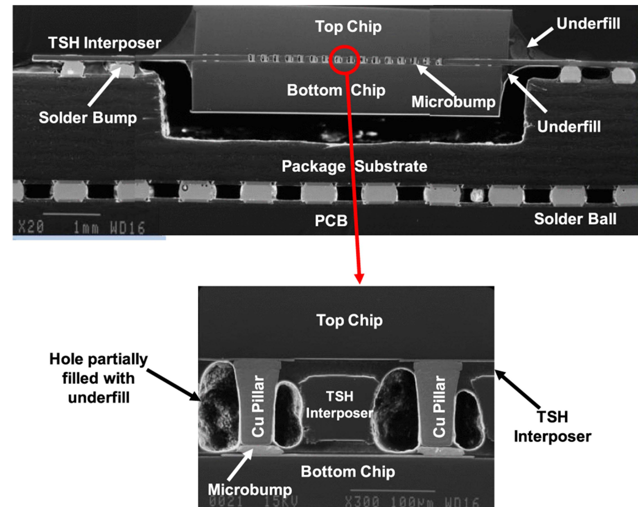

Fig. 7. Cross-sectional SEM image of the SiP (reproduced with permission from [193]).

cell positioning has been recognized to be an important design process to enable a high thermal conductivity path for heat dissipation [37], [78] and optimizing lateral heat transfer [188].

Several other approaches for thermal management related to TTSVs have also been explored. For example, graphene-based TTSVs and heat spreaders have been explored through simulations [189]. This proposed analysis has concluded that even if the carbon nanotube (CNT)-based 3-D IC structure is thermally superior to graphene [163], yet graphene-based finned TTSV structure may be preferred when higher interconnecting signal integrity is required. Since no experimental work was reported, the practical feasibility of incorporating graphene in the process flow remains to be established. Whereas a study based on the Nano-Engineered Computing Systems Technology (N3XT) stated that the carbon nanotube field-effect transistors (CNFETs) perform well in thermal and electrical aspects of a monolithic 3-D IC with higher electron mobility and good control over charge carrier concentration [190]. Other graphene-related aspects have also been reported, including the use of graphene as an efficient heat spreader [183], an interlayer in the form of multilayered graphene nanoribbons [191], or a TIM [184]. These studies have claimed that graphene may significantly enhance heat dissipation, even when used in small quantities [183], [184]. Heat dissipation using additional components integrated with 3-D IC such as thermally conductive sidewalls, interchip, or bottom plates has also been reported [192]. An improvement of around 40% compared with a conventional 3-D IC integrated with heat sink only has been reported. Replacement of conventional TSVs with simple copper wires and solders across through-silicon hole (TSH) interposers has been investigated [193]. Improved thermal cycling and electrical performance of 3-D ICs was reported with the use of TSH interposers on a fabricated test vehicle, in which the etched TSV is used for passing solid wire connections instead of being plated with metal. Fig. 7 displays the SEM cross-sectional image of the SiP which includes most of the key components such as TSH interposer, printed circuit board (PCB), package substrate, and top and bottom chips [193].

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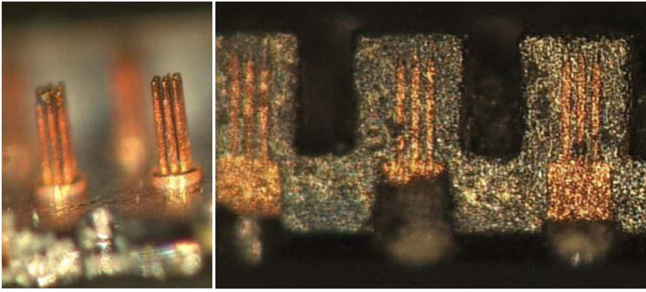

Fig. 8. TSV arrangement with micropin fin heatsink setup (reproduced with permission from [39]).

On the other hand, a concept of thermally isolating the sensitive IC components such as dynamic random-access memory (DRAM) from high-power heat-generating devices on chip was also developed. This concept has achieved the thermal isolation by implementing vacuum gaps in combination with noncontact chip-to-chip communications [181]; this study reported that the vacuum gaps enable the DRAM to operate at a temperature 47 °C lower than that of the conventional system. Another study includes arrangement of the TSVs in the shape of a ring around the device to be shielded from the surrounding heat generation [182] and successfully suppresses thermal coupling in a highly complex 3-D IC structures.

Several hybrid thermal management approaches have also been investigated for 3-D ICs, with the motivation of taking advantage of synergies that may exist between individual cooling mechanisms. For example, the performance of microfluid cooling in conjunction with TTSVs as a hybrid heat dissipation system has been investigated [38], [194]. While TTSVs help improve the capability of vertical heat conduction, microfluidic cooling helps remove heat from the 3-D IC structure using a heat transfer liquid as a heat carrier. This study claimed that the proposed hybrid system performs better than their individual mechanisms and achieves 56% savings in pump energy while maintaining higher heat dissipation capabilities [194]. Similar studies of hybrid thermal management combining microfluidic cooling and TTSVs have also reported similar enhancement in cooling performance of the system, either through numerical models [195], [196] or by fabrication and measurements on a customized experimental setup [197]. In another related study, thermal–electrical codesign of TSVs and microchannel cooling using micropin fin heat sink has been described [39]. Fig. 8 shows a picture of the TSV arrangement with micropin fin heatsink setup in this work [39]. An optimum design for micropin fin dimensions, TSV configuration, and coolant flow rate was carried out, resulting in 33% reduction in peak temperature in the circuit compared with a conventional air-cooled heat sink. A key challenge in such hybrid approaches is in accommodating a large number of TSVs in the 3-D IC along with efficient microchannel arrangements. Toward this, the feasibility of replacing TSVs with wireless interconnects has been explored [198]. This study has claimed greater efficiency in data communication and energy consumption using wireless interconnects compared with traditional TSVs.

Furthermore, a thermally active interposer along with microfluidic cooling has been proposed. It has been claimed that this approach of embedding microfluidic channels into the silicon interposer can minimize the number of layers of thermal interlayer materials used [199]. Similar studies on experimental measurements on a fabricated test vehicle have been reported to confirm the effectiveness of silicon interposers with TSV integrated microfluidic cooling [200] or micropin fin heatsink [201]. These measurements have shown that silicon interposer with microfluidic cooling has good thermal isolation between layers compared with conventional air cooling. Another method for thermal isolation of 3-D ICs using air gaps integrated in the microfluidic cooling along with a copper-spreader acting as a thermal bridge has been proposed [40], [202]. Using air gap isolation, this method claimed to reduce the peak temperature by 38.9 °C compared with a conventional design with just underfill and microbumps. An extension of this work was carried out by including mechanically flexible interconnects along with the air gap arrangement [203], based on which a 35.9% reduction in junction temperature of low power tier was achieved when compared with the conventional microbump-underfill-based design. Additionally, implementation of microgaps in conjunction with variable pin fin arrangements integrated in a single-phase microfluidic cooling system has been proposed. Experimental investigation of this approach and comparison against a comprehensive numerical model has been reported [204]. This article claimed that the hotspots can be suppressed using deionized water at 21.3 °C as coolant, and thus keeping the maximum temperature below 65 °C and maintaining pressure drop along the microchannels in acceptable range.

The decision of which thermal dissipation technique to implement for a certain 3-D IC must account for a variety of considerations, including the nature and complexity of the 3-D IC, number of chips, powermap, reliability, other characteristics, and cost. Custom requirements for niche applications such as military electronics must also be taken into consideration.

V. Future Outlook and Key Challenges

Despite much technological advances in multiple directions related to thermal management of 3-D ICs, as summarized in sections above, several technological challenges still remain. Some of these challenges are related to fundamental physical processes, while others are related to implementation of 3-D ICs for various applications.

There continues to be a need for analytical models for heat transfer in 3-D ICs that may be easily integrated with other tools for rapid temperature computation. This may help in both pre-silicon design and run-time performance optimization. Numerical simulation-based temperature computation is not appropriate for this purpose, since simulations often require commercial software to run on. In contrast, closed-form analytical solutions can be easily integrated with other codes. When such analytical solutions are available in a complicated form, such as an infinite series solution, a study of the trade-offs between accuracy and computation cost will be helpful. Benchmarking of such analytical solutions for temperature distribution with experimental measurements is also likely to be of much practical importance.

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Microfluidic cooling is one of the most promising thermal management techniques for 3-D ICs. There remain several key technological challenges associated with microfluidic cooling that must be addressed before the technology can be made mainstream. From a scientific perspective, understanding and optimally making use of the physics of liquid-to-gas phase change processes for improved heat removal is crucial, including scenarios such as thin-film evaporation. More work is needed on the integration of microfluidic cooling with electrical functions of the 3-D IC and in the use of enhanced surfaces such as micropin fins and offset strip fins. Practical challenges such as dynamic reallocation of microfluidic cooling resources to various tiers on a 3-D IC in response to load changes must be understood and addressed. Long-term reliability of microfluidic cooling needs to be better understood. It needs to be fully understood whether microfluidic cooling might influence existing failure mechanisms or cause entirely new ones. Droplet-based microfluidics, which is being investigated widely for analytical biochemistry, may also be useful for thermal management of 3-D ICs [205]. Thin-film evaporative cooling is another promising technology. In addition to fluid-based cooling, other novel thermal management mechanisms must also be investigated. In particular, solid-state cooling technologies such as thermoelectric cooling, while difficult to implement in a 3-D IC, offer a key advantage of no moving parts or moving fluid compared with microfluidic cooling. New materials innovations and investigation of compatibility with the existing materials are needed.

Microfluidic cooling can handle higher heat fluxes even under low pressures if the microchannel height is not limited due to maximum TSV height, since longer TSVs lead to higher signal latency. Additionally, high pressure drop is a key challenge with microfluidic cooling, which also results in undesirable mechanical stress. Such substantial pressure drops along the flow length also affect the saturation temperature of the coolant in a two-phase microfluidics cooling system, which results in objectionable interrupted flow behavior. Practical approaches may be needed for addressing such challenges, such as optimizing the flow path and using microchannels with hydrophobic inner surface.

Localized overheating commonly known as a hotspot is one of the prominent issues in 3-D ICs, which causes temperature nonuniformity across the chip and makes thermal management difficult with conventional IC cooling techniques. Dynamic hotspot prediction with the help of efficient thermal modeling techniques remains a critical challenge for 3-D IC thermal design and run-time performance management. Understanding the impact of TSV placement and 3-D IC floorplanning is critical. TSVs assist the heat dissipation if placed efficiently, achieving higher electrical performance along with excellent heat removal. Much work has been carried out on development of design and computation tools that combine electrical and thermal features. As thermal management technologies evolve, such tools need to be updated to accurately model such new thermal management approaches.

The TSV continues to be the central pillar of 3-D IC technology. Despite extensive work reported on the dual role of TSVs for thermal and electrical conduction, more work can be done to fully utilize the dual capabilities of a TSV. Theoretical modeling of the dual functions of a TSV is of much interest, as it may help understand the fundamentals of this challenging, multiphysics problem, and drive cooptimization.

Mechanical stress generation in a 3-D IC due to thermal gradients and dissimilar TCE of TSVs and silicon substrate remains a key practical challenge. The induced mechanical stress is influenced by a variety of factors, including material selection, TSV dimensions, pitch sizes, and overall floorplanning strategy. In addition to reliability, mechanical stress may also negatively impact signal transmission, redundant power dripping, and circuit timing. Increasingly accurate stress prediction tools need to be developed and used closely with other design tools.

Lately, there is a growing interest in monolithic 3-D (M3-D) integration to produce more efficient ICs having lower signal delay and reduced electrical interference [206], [207]. As a potential candidate for future vertically stacked complex ICs, multiple recent papers have attempted to improve and optimize this process [190], [208]–[211]. However, very limited amount of research is available on identifying and mitigating thermal management challenges in M3-D integration.

In general, early insertion of thermal management into the 3-D IC design process is critical, similar to traditional ICs. This will ensure early recognition and identification of thermal management challenges that may arise in next-generation 3-D ICs and help thermal management keep up with rapid advances in the manufacturing and packaging of 3-D ICs expected in the coming years.

VI. Conclusion

3-D ICs have attracted a considerable volume of research literature in a variety of subdisciplines within electrical, computer, and mechanical engineering. This review article summarizes the key developments pertaining to heat transfer in 3-D ICs. The overall goal of this article has been to summarize key research developments reported in the areas of thermal modeling, thermal–electrical codesign, and thermal management of a 3-D IC. It is expected that the summary of the current state-of-the-art and the discussion on future outlook in these areas will help researchers in academia and industry working on these and related challenges pertaining to 3-D ICs.

References

[1] I. M. Ross, "The invention of the transistor," *Proc. IEEE*, vol. 86, no. 1, pp. 7–28, 1998.

[2] C. A. Mack, "Fifty years of Moore's law," *IEEE Trans. Semicond. Manuf.*, vol. 24, no. 2, pp. 202–207, May 2011.

[3] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore," white paper. International Technology Roadmap for Semiconductors (ITRS) Report. Accessed: Dec. 9, 2020. [Online]. Available: http://www.itrs2.net/uploads/4/9/7/7/49775221/irc-itrs-mtm-v2_3.pdf

[4] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[5] R. S. Patti, "Three-dimensional integrated circuits and the future of system-on-chip designs," *Proc. IEEE*, vol. 94, no. 6, pp. 1214–1224, Jun. 2006.

Authorized licensed use limited to: University of Texas at Arlington. Downloaded on May 17,2021 at 22:15:35 UTC from IEEE Xplore. Restrictions apply.

[6] A. W. Topol *et al.*, "Three-dimensional integrated circuits," *IBM J. Res. Develop.*, vol. 50, nos. 4–5, pp. 491–506, Jul./Sep. 2006.

[7] Y. Chen, D. Niu, Y. Xie, and K. Chakrabarty, "Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 471–476.

[8] S. M. Alam, R. E. Jones, S. Pozder, R. Chatterjee, S. Rauf, and A. Jain, "Interstratum connection design considerations for cost-effective 3-D system integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 3, pp. 450–460, Mar. 2010.

[9] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Introduction," in *Three-dimensional Integrated Circuit Design*, 2nd ed., V. F. Pavlidis, I. Savidis, and E. G. Friedman, Eds. Boston, MA, USA: Elsevier, 2017, pp. 1–14.

[10] W. R. Davis *et al.*, "Demystifying 3D ICs: The pros and cons of going vertical," *IEEE Design Test Comput.*, vol. 22, no. 6, pp. 498–510, Jun. 2005.

[11] K. Cao, J. Zhou, T. Wei, M. Chen, S. Hu, and K. Li, "A survey of optimization techniques for thermal-aware 3D processors," *J. Syst. Archit.*, vol. 97, pp. 397–415, Aug. 2019.

[12] B. Rajendran, "Sequential 3D IC fabrication-challenges and prospects," in *Proc. VLSI Multilevel Interconnect Conf.*, 2006, pp. 57–64.

[13] S. Wong, A. El-Gamal, P. Griffin, Y. Nishi, F. Pease, and J. Plummer, "Monolithic 3D integrated circuits," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, 2007, pp. 1–4.

[14] S. S. Wong and A. E. Gamal, "The prospect of 3D-IC," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 445–448.

[15] A. Chaudhuri *et al.*, "Advances in design and test of monolithic 3-D ICs," *IEEE Des. Test*, vol. 37, no. 4, pp. 92–100, Apr. 2020.

[16] S. Panth, S. Samal, Y. S. Yu, and S. K. Lim, "Design challenges and solutions for ultra-high-density monolithic 3D ICs," *J. Inf. Commun. Converg. Eng.*, vol. 12, no. 3, pp. 186–192, Sep. 2014.

[17] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Manufacturing technologies for three-dimensional integrated circuits," in *Three-Dimensional Integrated Circuit Design*, 2nd ed., V. F. Pavlidis, I. Savidis, and E. G. Friedman, Eds. Boston, MA, USA: Elsevier, 2017, pp. 37–65.

[18] A. K. Henning, B. Rajendran, B. Cronquist, and Z. Or-Bach, "Thermal considerations for monolithic integration of three-dimensional integrated circuits," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (SS)*, Oct. 2013, pp. 1–2.

[19] D. C. Sekar and Z. Or-Bach, "Monolithic 3D-ICs with single crystal silicon layers," in *Proc. IEEE IEEE Int. 3D Syst. Integr. Conf. (3DIC) Int.*, Jan. 2012, pp. 1–2.

[20] P. R. Morrow, C.-M. Park, S. Ramanathan, M. J. Kobrinsky, and M. Harmes, "Three-dimensional wafer stacking via Cu-Cu bonding integrated with 65-nm strained-Si/low-K CMOS technology," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 335–337, May 2006.

[21] A. W. Topol *et al.*, "Enabling SOI-based assembly technology for three-dimensional (3D) integrated circuits (ICs)," in *IEDM Tech. Dig.*, Dec. 2005, pp. 352–355.

[22] K. Sakuma *et al.*, "Bonding technologies for chip level and wafer level 3D integration," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 647–654.

[23] B. Black, D. W. Nelson, C. Webb, and N. Samra, "3D processing technology and its impact on iA32 microprocessors," in *Proc. IEEE Int. Conf. Comput. Des., VLSI Comput. Processors (ICCD)*, 2004, pp. 316–318.

[24] S. Hamdioui, "Yield improvement and test cost reduction for TSV based 3D stacked ICs," in *Proc. 6th Int. Conf. Design Technol. Integr. Syst. Nanosc. Era (DTIS)*, Apr. 2011, p. 1.

[25] S. M. Alam, R. E. Jones, S. Pozder, and A. Jain, "Die/wafer stacking with reciprocal design symmetry (RDS) for mask reuse in three-dimensional (3D) integration technology," in *Proc. 10th Int. Symp. Qual. Electron. Design*, Mar. 2009, pp. 569–575.

[26] B. Kim, C. Sharbono, T. Ritzdorf, and D. Schmauch, "Factors affecting copper filling process within high aspect ratio deep vias for 3D chip stacking," in *Proc. 56th Electron. Compon. Technol. Conf.*, 2006, pp. 838–843.

[27] S. Pasricha, "Exploring serial vertical interconnects for 3D ICs," in *Proc. 46th Annu. Design Autom. Conf. ZZZ (DAC)*, 2009, p. 581.

[28] A. R. Mirza, "One micron precision, wafer-level aligned bonding for interconnect, MEMS and packaging applications," in *Proc. 50th Electron. Compon. Technol. Conf.*, 2000, pp. 676–680.

[29] X. Dong and Y. Xie, "System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs)," in *Proc. Asia South Pacific Design Autom. Conf.*, Jan. 2009, pp. 234–241.

[30] S. G. Kandlikar, "Review and projections of integrated cooling systems for three-dimensional integrated circuits," *J. Electron. Packag.*, vol. 136, no. 2, pp. 1–11, Jun. 2014.

[31] M. M. Sabry, A. K. Coskun, D. Atienza, T. Š. Rosing, and T. Brunschwiler, "Energy-efficient multiobjective thermal control for liquid-cooled 3-D stacked architectures," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 12, pp. 1883–1896, Dec. 2011.

[32] D. Sekar *et al.*, "A 3D-IC technology with integrated microchannel cooling," in *Proc. Int. Interconnect Technol. Conf.*, Jun. 2008, pp. 13–15.

[33] G. Luo, Y. Shi, and J. Cong, "An analytical placement framework for 3-D ICs and its extension on thermal awareness," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 32, no. 4, pp. 510–523, Apr. 2013.

[34] B. Goplen and S. Sapatnekar, "Efficient thermal placement of standard cells in 3D ICs using a force directed approach," in *Proc. Int. Conf. Comput. Aided Design (ICCAD)*, Nov. 2003, pp. 86–89.

[35] Y. Zhang *et al.*, "Coupled electrical and thermal 3D IC centric microfluidic heat sink design and technology," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May 2011, pp. 2037–2044.

[36] J. H. Lau and T. G. Yue, "Thermal management of 3D IC integration with TSV (through silicon via)," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 635–640.

[37] P.-Y. Hsu, H.-T. Chen, and T. Hwang, "Stacking signal TSV for thermal dissipation in global routing for 3D IC," in *Proc. 18th Asia South Pacific Design Autom. Conf. (ASP-DAC)*, Jan. 2013, pp. 699–704.

[38] B. Shi, A. Srivastava, and A. Bar-Cohen, "Hybrid 3D-IC cooling system using micro-fluidic cooling and thermal TSVs," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI*, Aug. 2012, pp. 33–38.

[39] Y. Zhang, A. Dembla, and M. S. Bakir, "Silicon micropin-fin heat sink with integrated TSVs for 3-D ICs: Tradeoff analysis and experimental testing," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 11, pp. 1842–1850, Nov. 2013.

[40] Y. Zhang, Y. Zhang, and M. S. Bakir, "Thermal design and constraints for heterogeneous integrated chip stacks and isolation technology using air gap and thermal bridge," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 12, pp. 1914–1924, Dec. 2014.

[41] V. Venkatadri, B. Sammakia, K. Srihari, and D. Santos, "A review of recent advances in thermal management in three dimensional chip stacks in electronic systems," *J. Electron. Packag.*, vol. 133, no. 4, Dec. 2011.

[42] C. Green *et al.*, "A review of two-phase forced cooling in three-dimensional stacked electronics: Technology integration," *J. Electron. Packag.*, vol. 137, no. 4, pp. 040802:1–040802:9, Dec. 2015.

[43] S. S. Sapatnekar, "Addressing thermal and power delivery bottlenecks in 3D circuits," in *Proc. Asia South Pacific Design Autom. Conf.*, Jan. 2009, pp. 423–428.

[44] A. Rahman and R. Reif, "Thermal analysis of three-dimensional (3-D) integrated circuits (ICs)," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2001, vol. 19, no. 4, pp. 157–159.

[45] G. Nagy, P. Horváth, L. Pohl, and A. Poppe, "Advancing the thermal stability of 3D ICs using logi-thermal simulation," *Microelectron. J.*, vol. 46, no. 12, pp. 1114–1120, Dec. 2015.

[46] S. Liu, C. Wang, Z. Yu, W. Tang, and W. Zhuang, "Thermal-WLP: A transient thermal simulation method based on weighted Laguerre polynomials for 3-D ICs," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 3, pp. 405–411, Mar. 2017.

[47] L. Jani and A. Poppe, "Adaptive co-simulation of functional-thermal behaviour of integrated circuits," in *Proc. 23rd Int. Workshop Thermal Investigations ICs Syst. (THERMINIC)*, Sep. 2017, pp. 1–8.

[48] S. H. Pan, N. Chang, and J. Zheng, "A new methodology for IC-package thermal co-analysis in 3D IC environment," in *Proc. IEEE Electr. Design Adv. Package Syst. Symp.*, Dec. 2010, pp. 1–4.

[49] L. Lu and L. Chiou, "Temperature gradient-aware thermal simulator for three-dimensional integrated circuits," *IET Comput. Digit. Techn.*, vol. 11, no. 5, pp. 190–196, Sep. 2017.

[50] K. O. Petrosyants and N. I. Ryabov, "Quasi-3D thermal simulation of integrated circuit systems in packages," *Energies*, vol. 13, no. 12, p. 3054, Jun. 2020.

[51] L. Choobineh and A. Jain, "Determination of temperature distribution in three-dimensional integrated circuits (3D ICs) with unequally-sized die," *Appl. Thermal Eng.*, vol. 56, nos. 1–2, pp. 176–184, Jul. 2013.

[52] C. Santos, P. Vivet, and R. Reis, "Thermal impact of 3D stacking and die thickness: Analysis and characterization of a memory-on-logic 3D circuit," in *Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2014, pp. 718–721.

Authorized licensed use limited to: University of Texas at Arlington. Downloaded on May 17,2021 at 22:15:35 UTC from IEEE Xplore. Restrictions apply.

[53] S. Rangarajan, Y. Hadad, L. Choobineh, and B. Sammakia, "Minimizing temperature nonuniformity by optimal arrangement of hotspots in vertically stacked three-dimensional integrated circuits," *J. Electron. Packag.*, vol. 142, no. 4, pp. 1–9, Dec. 2020.

[54] C.-P. Chen, Y. Weng, and G. Subbarayan, "Topology optimization for efficient heat removal in 3D packages," in *Proc. 15th IEEE Intersociety Conf. Thermal Thermomechanical Phenomena Electron. Syst. (ITherm)*, May 2016, pp. 238–244.

[55] T. R. Harris *et al.*, "Thermal simulation of heterogeneous GaN/InP/silicon 3DIC stacks," in *Proc. Int. 3D Syst. Integr. Conf. (3DIC)*, Aug. 2015, pp. TS10.2.1–TS10.2.4.

[56] A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler, and D. Atienza, "3D-ICE: Fast compact transient thermal modeling for 3D ICs with inter-tier liquid cooling," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 463–470.

[57] K.-J. Wang, H.-C. Sun, and Z.-L. Pan, "An analytical thermal model for three-dimensional integrated circuits with integrated micro-channel cooling," *Thermal Sci.*, vol. 21, no. 4, pp. 1601–1606, 2017.

[58] P. Zając, "Compact thermal modelling tool for fast design space exploration of 3D ICs with integrated microchannels," *Energies*, vol. 13, no. 9, p. 2217, May 2020.

[59] A. Jain, R. E. Jones, R. Chatterjee, and S. Pozder, "Analytical and numerical modeling of the thermal performance of three-dimensional integrated circuits," *IEEE Trans. Compon., Packag., Technol.*, vol. 33, no. 1, pp. 56–63, Mar. 2010.

[60] L. Han and Z. Tong, "A thermal resistance network model based on three-dimensional structure," *Measurement*, vol. 133, pp. 439–443, Feb. 2019.

[61] X. Hu *et al.*, "Thermal resistance analysis for a high power 3D integrated RF module based on TSV interposer," in *Proc. IEEE 21st Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2019, pp. 406–412.

[62] L. Choobineh, J. Jones, and A. Jain, "Experimental and numerical investigation of interdie thermal resistance in three-dimensional integrated circuits," *J. Electron. Packag.*, vol. 139, no. 2, pp. 1–6, Jun. 2017.

[63] E. G. Colgan *et al.*, "Measurement of microbump thermal resistance in 3D chip stacks," in *Proc. 28th Annu. IEEE Semiconductor Thermal Meas. Manage. Symp. (SEMI-THERM)*, Mar. 2012, pp. 1–7.

[64] H. Oprins *et al.*, "Characterization and benchmarking of the low intertier thermal resistance of three-dimensional hybrid Cu/dielectric wafer-to-wafer bonding," *J. Electron. Packag.*, vol. 139, no. 1, pp. 1–9, Mar. 2017.

[65] W. Zhu, G. Dong, and Y. Yang, "Thermal-aware modeling and analysis for a power distribution network including through-silicon-vias in 3-D ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 38, no. 7, pp. 1278–1290, Jul. 2019.

[66] C. Xiao, H. He, J. Li, S. Cao, and W. Zhu, "An effective and efficient numerical method for thermal management in 3D stacked integrated circuits," *Appl. Thermal Eng.*, vol. 121, pp. 200–209, Jul. 2017.

[67] Y. Pi, N. Wang, J. Chen, M. Miao, Y. Jin, and W. Wang, "Anisotropic equivalent thermal conductivity model for efficient and accurate full-chip-scale numerical simulation of 3D stacked IC," *Int. J. Heat Mass Transf.*, vol. 120, pp. 361–378, May 2018.

[68] S. Priyadarshi, W. R. Davis, and P. D. Franzon, "Pathfinder3D: A framework for exploring early thermal tradeoffs in 3DIC," in *Proc. IEEE Int. Conf. IC Design Technol.*, May 2014, pp. 1–6.

[69] H. Yan, Q. Zhou, and X. Hong, "Thermal aware placement in 3D ICs using quadratic uniformity modeling approach," *Integration*, vol. 42, no. 2, pp. 175–180, Feb. 2009.

[70] S. G. Kandlikar and A. Ganguly, "Fundamentals of heat dissipation in 3D IC packaging and thermal-aware design," in *3D Microelectronic Packaging* (Springer Series in Advanced Microelectronics), vol. 64. Singapore: Springer, 2021, pp. 369–395.

[71] J. Cong and G. Luo, "Advances and challenges in 3D physical design," *IPSJ Trans. Syst. LSI Design Methodology*, vol. 3, pp. 2–18, 2010.

[72] K. N. Dang, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "A thermal-aware on-line fault tolerance method for TSV lifetime reliability in 3D-NoC systems," *IEEE Access*, vol. 8, pp. 166642–166657, 2020.

[73] Q. Zou, E. Kursun, and Y. Xie, "Thermomechanical stress-aware management for 3-D IC designs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 9, pp. 2678–2682, Sep. 2017.

[74] Q. Xu and S. Chen, "Fast thermal analysis for fixed-outline 3D floorplanning," *Integration*, vol. 59, pp. 157–167, Sep. 2017.

[75] T. Ni *et al.*, "Temperature-aware floorplanning for fixed-outline 3D ICs," *IEEE Access*, vol. 7, pp. 139787–139794, 2019.

[76] *HotSpot 6.0 Temperature Modeling Tool.* Accessed: Jul. 16, 2020. [Online]. Available: http://lava.cs.virginia.edu/HotSpot/versions.htm

[77] D. H. Kim, K. Athikulwongse, and S. K. Lim, "Study of through-silicon-via impact on the 3-D stacked IC layout," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 5, pp. 862–874, May 2013.

[78] K. Athikulwongse, M. Ekpanyapong, and S. K. Lim, "Exploiting die-to-die thermal coupling in 3-D IC placement," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 10, pp. 2145–2155, Oct. 2014.

[79] R. Dash, A. Majumdar, V. Pangracious, A. K. Turuk, and J. L. Risco-Martin, "ATAR: An adaptive thermal-aware routing algorithm for 3-D network-on-chip systems," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 12, pp. 2122–2129, Dec. 2018.

[80] S.-Y. Lin, T.-C. Yin, H.-Y. Wang, and A.-Y. Wu, "Traffic-and thermal-aware routing for throttled three-dimensional network-on-chip systems," in *Proc. Int. Symp. VLSI Design, Autom. Test*, Apr. 2011, pp. 1–4.

[81] F. Liu, H. Gu, and Y. Yang, "DTBR: A dynamic thermal-balance routing algorithm for network-on-chip," *Comput. Electr. Eng.*, vol. 38, no. 2, pp. 270–281, Mar. 2012.

[82] J. Wang, H. Gu, Y. Yang, and K. Wang, "An energy- and buffer-aware fully adaptive routing algorithm for network-on-chip," *Microelectron. J.*, vol. 44, no. 2, pp. 137–144, Feb. 2013.

[83] P. Sivakumar, K. Pandiaraj, and K. JeyaPrakash, "Optimization of thermal aware multilevel routing for 3D IC," *Anal. Integr. Circuits Signal Process.*, vol. 103, no. 1, pp. 131–142, Apr. 2020.

[84] Y. Satomi, K. Hachiya, T. Kanamoto, R. Watanabe, and A. Kurokawa, "Thermal placement on PCB of components including 3D ICs," *IEICE Electron. Exp.*, vol. 17, no. 3, 2020, Art. no. 20190737.

[85] J. Cong, G. Luo, J. Wei, and Y. Zhang, "Thermal-aware 3D IC placement via transformation," in *Proc. Asia South Pacific Design Autom. Conf.*, Jan. 2007, pp. 780–785.

[86] Z. Ren, A. Alqahtani, N. Bagherzadeh, and J. Lee, "Thermal TSV optimization and hierarchical floorplanning for 3-D integrated circuits," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 10, no. 4, pp. 599–610, Apr. 2020.

[87] N. Shahabinejad and H. Beitollahi, "Q-thermal: A Q-learning-based thermal-aware routing algorithm for 3-D network on-chips," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 10, no. 9, pp. 1482–1490, Sep. 2020.

[88] R. Dash, J. L. Risco-Martin, A. K. Turuk, J. L. Ayala, V. Pangracious, and A. Majumdar, "A bio-inspired hybrid thermal management approach for 3-D network-on-chip systems," *IEEE Trans. Nanobiosci.*, vol. 16, no. 8, pp. 727–743, Dec. 2017.

[89] P. Budhathoki, A. Henschel, and I. A. M. Elfadel, "Thermal-driven 3D floorplanning using localized TSV placement," in *Proc. IEEE Int. Conf. IC Design Technol.*, May 2014, pp. 1–4.

[90] J. M. Minz, E. Wong, M. Pathak, and S. K. Lim, "Placement and routing for 3-D system-on-package designs," *IEEE Trans. Compon., Packag., Technol.*, vol. 29, no. 3, pp. 644–657, Sep. 2006.

[91] B. Goplen and S. Sapatnekar, "Placement of 3D ICs with thermal and interlayer via considerations," in *Proc. 44th ACM/IEEE Design Autom. Conf.*, Jun. 2007, pp. 626–631.

[92] Y.-J. Lee and S. Kyu Lim, "Co-optimization and analysis of signal, power, and thermal interconnects in 3-D ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 11, pp. 1635–1648, Nov. 2011.

[93] M. Healy *et al.*, "Multiobjective microarchitectural floorplanning for 2-D and 3-D ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no. 1, pp. 38–52, Jan. 2007.

[94] M. Pathak and S. Kyu Lim, "Performance and thermal-aware Steiner routing for 3-D stacked ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 9, pp. 1373–1386, Sep. 2009.

[95] A. Jain, S. M. Alam, S. Pozder, and R. E. Jones, "Thermal–electrical co-optimisation of floorplanning of three-dimensional integrated circuits under manufacturing and physical design constraints," *IET Comput. Digit. Techn.*, vol. 5, no. 3, p. 169, 2011.

[96] Y. Zhao, C. Hao, and T. Yoshimura, "TSV assignment of thermal and wirelength optimization for 3D-IC routing," in *Proc. 28th Int. Symp. Power Timing Modeling, Optim. Simulation (PATMOS)*, Jul. 2018, pp. 155–162.

[97] Y. A. Durrani, "Power and thermal modeling approach for homogeneously stacked butterfly fat tree architecture in 3D ICs," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. 31, no. 5, p. e2330, Sep. 2018.

[98] C. Serafy, A. Bar-Cohen, A. Srivastava, and D. Yeung, "Unlocking the true potential of 3-D CPUs with microfluidic cooling," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 4, pp. 1515–1523, Apr. 2016.

Authorized licensed use limited to: University of Texas at Arlington. Downloaded on May 17,2021 at 22:15:35 UTC from IEEE Xplore. Restrictions apply.

[99] Z. Yang and A. Srivastava, "Physical design of 3D FPGAs embedded with micro-channel-based fluidic cooling," in *Proc. ACM/SIGDA Int. Symp. Field-Program. Gate Arrays*, Feb. 2016, pp. 54–63.

[100] T. Lu, F. Zhang, and J.-M. Jin, "Multiphysics simulation of 3-D ICs with integrated microchannel cooling," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 11, pp. 1620–1629, Nov. 2016.

[101] Z. Yang and A. Srivastava, "Physical co-design for micro-fluidically cooled 3D ICs," in *Proc. 15th IEEE Intersociety Conf. Thermal Thermomechanical Phenomena Electron. Syst. (ITherm)*, May 2016, pp. 1373–1380.

[102] F. Zanini, M. M. Sabry, D. Atienza, and G. De Micheli, "Hierarchical thermal management policy for high-performance 3D systems with liquid cooling," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 2, pp. 88–101, Jun. 2011.

[103] C. Serafy, Z. Yang, A. Srivastava, Y. Hu, and Y. Joshi, "Thermoelectric codesign of 3-D CPUs and embedded microfluidic pin-fin heatsinks," *IEEE Des. Test. IEEE Des. Test. Comput.*, vol. 33, no. 2, pp. 40–48, Apr. 2016.

[104] K. H. Lu, X. Zhang, S.-K. Ryu, J. Im, R. Huang, and P. S. Ho, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 630–634.

[105] Y. Dai, M. Zhang, F. Qin, P. Chen, and T. An, "Effect of silicon anisotropy on interfacial fracture for three dimensional through-silicon-via (TSV) under thermal loading," *Eng. Fract. Mech.*, vol. 209, pp. 274–300, Mar. 2019.

[106] S. K. Marella and S. S. Sapatnekar, "A holistic analysis of circuit performance variations in 3-D ICs with thermal and TSV-induced stress considerations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 7, pp. 1308–1321, Jul. 2015.

[107] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim, "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC," *Commun. ACM*, vol. 57, no. 1, pp. 107–115, Jan. 2014.

[108] M. P. D. Sai, H. Yu, Y. Shang, C. Seng Tan, and S. Kyu Lim, "Reliable 3-D clock-tree synthesis considering nonlinear capacitive TSV model with electrical–thermal–mechanical coupling," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 11, pp. 1734–1747, Nov. 2013.

[109] A. P. Karmarkar, X. Xu, and V. Moroz, "Performanace and reliability analysis of 3D-integration structures employing through silicon via (TSV)," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2009, pp. 682–687.

[110] T. Jiang, J. Im, R. Huang, and P. S. Ho, "Through-silicon via stress characteristics and reliability impact on 3D integrated circuits," *MRS Bull.*, vol. 40, no. 3, pp. 248–256, Mar. 2015.

[111] N. Minas *et al.*, "Test structures for characterization of thermal-mechanical stress in 3D stacked IC for analog design," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, Mar. 2010, pp. 140–144.

[112] A. S. Budiman *et al.*, "Measurement of stresses in cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectron. Rel.*, vol. 52, no. 3, pp. 530–533, Mar. 2012.

[113] N. Ranganathan, K. Prasad, N. Balasubramanian, and K. L. Pey, "A study of thermo-mechanical stress and its impact on through-silicon vias," *J. Micromech. Microeng.*, vol. 18, no. 7, Jul. 2008, Art. no. 075018.

[114] L. J. Ladani, "Numerical analysis of thermo-mechanical reliability of through silicon vias (TSVs) and solder interconnects in 3-dimensional integrated circuits," *Microelectron. Eng.*, vol. 87, no. 2, pp. 208–215, Feb. 2010.

[115] J. Pang and J. Wang, "The thermal stress analysis for IC integrations with TSV interposer by complement sector models," *J. Electron. Mater.*, vol. 43, no. 9, pp. 3423–3435, Sep. 2014.

[116] A. Benali, M. Bouya, M. Faqir, A. El Amrani, M. Ghogho, and A. Benabdellah, "Through glass via thermomechanical analysis: Geometrical parameters effect on thermal stress," in *Proc. 8th IEEE Design Test Symp.*, Dec. 2013, pp. 1–5.

[117] J. Zhang, M. O. Bloomfield, J.-Q. Lu, R. J. Gutmann, and T. S. Cale, "Modeling thermal stresses in 3-D IC interwafer interconnects," *IEEE Trans. Semicond. Manuf.*, vol. 19, no. 4, pp. 437–448, Nov. 2006.

[118] T. Kinoshita *et al.*, "Thermal stresses of through silicon vias and Si chips in three dimensional system in package," *J. Electron. Packag.*, vol. 134, no. 2, pp. 3–6, Jun. 2012.

[119] E. J. Cheng and Y.-L. Shen, "Thermal expansion behavior of through-silicon-via structures in three-dimensional microelectronic packaging," *Microelectron. Rel.*, vol. 52, no. 3, pp. 534–540, Mar. 2012.

[120] R. W. Johnson and Y.-L. Shen, "Analysis of thermal stress and its influence on carrier mobility in three-dimensional microelectronic chip stack," *J. Electron. Packag.*, vol. 137, no. 2, pp. 1–11, Jun. 2015.

[121] S.-K. Ryu, K.-H. Lu, X. Zhang, J.-H. Im, P. S. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon vias for 3-D interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 35–43, Mar. 2011.

[122] H. Zhou, H. Zhu, T. Cui, D. Z. Pan, D. Zhou, and X. Zeng, "Thermal stress and reliability analysis of TSV-based 3-D ICs with a novel adaptive strategy finite element method," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 7, pp. 1312–1325, Jul. 2018.

[123] X. Yang, J. Tan, B. Zhou, D. Hua, G. Tang, and T. Qiao, "Thermal-stress analysis of 3D-IC based on artificial neural network," in *Proc. IEEE 4th Int. Conf. Cloud Comput. Big Data Anal. (ICCCBDA)*, Apr. 2019, pp. 105–110.

[124] H. Wang *et al.*, "Runtime stress estimation for three-dimensional IC reliability management using artificial neural network," *ACM Trans. Design Autom. Electron. Syst.*, vol. 24, no. 6, pp. 1–29, Nov. 2019.

[125] H. Wang, D. Huang, R. Liu, C. Zhang, H. Tang, and Y. Yuan, "STREAM: Stress and thermal aware reliability management for 3-D ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 38, no. 11, pp. 2058–2071, Nov. 2019.

[126] H. Sun, Y. Pi, W. Wang, J. Chen, and Y. Jin, "Groove structure for stress releasing around TSV," in *Proc. 14th Int. Conf. Electron. Packag. Technol.*, Aug. 2013, pp. 965–967.

[127] S. Islam and I. Abdel-Motaleb, "Numerical analysis of liquid cooling of 3D-ICs using embedded channels," in *Proc. IEEE Int. Conf. Electro Inf. Technol. (EIT)*, Jul. 2020, pp. 233–238.

[128] S. Islam and I. Abdel-Motaleb, "Thermal stress analysis of liquid-cooled 3D-ICs," in *Proc. IEEE Int. Conf. Electro Inf. Technol. (EIT)*, Jul. 2020, pp. 132–135.

[129] B. Ding, Z.-H. Zhang, L. Gong, C.-Y. Zhu, and M.-H. Xu, "Coupling management optimization of temperature and thermal stress inside 3D-IC with multi-cores and various power density," *Int. Commun. Heat Mass Transf.*, vol. 120, Jan. 2021, Art. no. 105021.

[130] K. Athikulwongse, A. Chakraborty, J.-S. Yang, D. Z. Pan, and S. K. Lim, "Stress-driven 3D-IC placement with TSV keep-out zone and regularity study," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 669–674.

[131] T. Lu, Z. Yang, and A. Srivastava, "Post-placement optimization for thermal-induced mechanical stress reduction," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, Jul. 2016, pp. 158–163.

[132] S.-K. Ryu *et al.*, "Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects," *J. Appl. Phys.*, vol. 111, no. 6, Mar. 2012, Art. no. 063513.

[133] T. Jiang, S.-K. Ryu, Q. Zhao, J. Im, R. Huang, and P. S. Ho, "Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias," *Microelectron. Rel.*, vol. 53, no. 1, pp. 53–62, Jan. 2013.

[134] C. S. Wong, N. S. Bennett, D. Manessis, A. Danilewsky, and P. J. McNally, "Non-destructive laboratory-based X-ray diffraction mapping of warpage in Si die embedded in IC packages," *Microelectron. Eng.*, vol. 117, pp. 48–56, Apr. 2014.

[135] J. Dai, P. Mukundhan, C. Kim, and H. J. Maris, "Analysis of a picosecond ultrasonic method for measurement of stress in a substrate," *J. Appl. Phys.*, vol. 119, no. 10, Mar. 2016, Art. no. 105705.

[136] P. S. Ho and T. Kwok, "Electromigration in metals," *Rep. Prog. Phys.*, vol. 52, no. 3, pp. 301–348, Mar. 1989.

[137] J. Pak, S. K. Lim, and D. Z. Pan, "Electromigration study for multiscale power/ground vias in TSV-based 3-D ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 12, pp. 1873–1885, Dec. 2014.

[138] T. Lu, Z. Yang, and A. Srivastava, "Electromigration-aware placement for 3D-ICs," in *Proc. 17th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2016, pp. 35–40.

[139] T. Lu and A. Srivastava, "Electrical-thermal-reliability co-design for TSV-based 3D-ICs," *Thermal Manage.*, vol. 53, no. 9, pp. 1–30, 2015.

[140] S. Wang, Y. Yin, C. Hu, and P. Rezai, "3D integrated circuit cooling with microfluidics," *Micromachines*, vol. 9, no. 6, p. 287, Jun. 2018.

[141] S. G. Kandlikar and A. V. Bapat, "Evaluation of jet impingement, spray and microchannel chip cooling options for high heat flux removal," *Heat Transf. Eng.*, vol. 28, no. 11, pp. 911–923, Nov. 2007.

[142] D. B. Tuckerman and R. F. W. Pease, "High-performance heat sinking for VLSI," *IEEE Electron Device Lett.*, vol. 2, no. 5, pp. 126–129, May 1981.

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[143] H. Zhu, F. Hu, H. Zhou, D. Z. Pan, D. Zhou, and X. Zeng, "Interlayer cooling network design for high-performance 3D ICs using channel patterning and pruning," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 4, pp. 770–781, Apr. 2018.

[144] L. K. Hwang, B. Kwon, and M. D. F. Wong, "Optimization of liquid cooling microchannel in 3D IC using complete converging and diverging channel models," in *Proc. 18th IEEE Intersociety Conf. Thermal Thermomechanical Phenomena Electron. Syst. (ITherm)*, May 2019, pp. 1197–1203.

[145] H. Qian, C.-H. Chang, and H. Yu, "An efficient channel clustering and flow rate allocation algorithm for non-uniform microfluidic cooling of 3D integrated circuits," *Integration*, vol. 46, no. 1, pp. 57–68, Jan. 2013.

[146] D. Lorenzini-Gutierrez and S. G. Kandlikar, "Variable fin density flow channels for effective cooling and mitigation of temperature nonuniformity in three-dimensional integrated circuits," *J. Electron. Packag.*, vol. 136, no. 2, pp. 1–11, Jun. 2014.

[147] B. Ding, Z.-H. Zhang, L. Gong, M.-H. Xu, and Z.-Q. Huang, "A novel thermal management scheme for 3D-IC chips with multi-cores and high power density," *Appl. Thermal Eng.*, vol. 168, Mar. 2020, Art. no. 114832.

[148] J.-M. Koo, S. Im, L. Jiang, and K. E. Goodson, "Integrated microchannel cooling for three-dimensional electronic circuit architectures," *J. Heat Transf.*, vol. 127, no. 1, pp. 49–58, Jan. 2005.

[149] J.-Y. Park, L. Peng, and J.-W. Choi, "Critical heat flux limiting the effective cooling performance of two-phase cooling with an interlayer microchannel," *Microsyst. Technol.*, vol. 25, no. 7, pp. 2831–2840, Jul. 2019.

[150] A. Fourmigue, G. Beltrame, and G. Nicolescu, "Transient thermal simulation of liquid-cooled 3-D circuits," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 9, pp. 1349–1360, Sep. 2016.

[151] P. Zając and A. Napieralski, "Novel thermal model of microchannel cooling system designed for fast simulation of liquid-cooled ICs," *Microelectron. Rel.*, vol. 87, pp. 245–258, Aug. 2018.

[152] M. Németh, G. Takács, L. Jani, and A. Poppe, "Compact modeling approach for microchannel cooling and its validation," *Microsyst. Technol.*, vol. 24, no. 1, pp. 419–431, Jan. 2018.

[153] D. Kearney, T. Hilt, and P. Pham, "A numerical hydrodynamic and thermal characterization of an inter-strata liquid cooling solution for 3D ICs," *Microsyst. Technol.*, vol. 18, no. 2, pp. 225–235, Feb. 2012.

[154] H. Mizunuma, Y.-C. Lu, and C.-L. Yang, "Thermal modeling and analysis for 3-D ICs with integrated microchannel cooling," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 9, pp. 1293–1306, Sep. 2011.

[155] D. Kearney, T. Hilt, and P. Pham, "A liquid cooling solution for temperature redistribution in 3D IC architectures," *Microelectron. J.*, vol. 43, no. 9, pp. 602–610, Sep. 2012.

[156] B. Shi and A. Srivastava, "Optimized micro-channel design for stacked 3-D-ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 1, pp. 90–100, Jan. 2014.

[157] B. Shi, A. Srivastava, and P. Wang, "Non-uniform micro-channel design for stacked 3D-ICs," in *Proc. 48th Design Autom. Conf. (DAC)*, 2011, pp. 658–663.

[158] G. Chen, J. Kuang, Z. Zeng, H. Zhang, E. F. Y. Young, and B. Yu, "Minimizing thermal gradient and pumping power in 3D IC liquid cooling network design," in *Proc. 54th Annu. Design Autom. Conf.*, Jun. 2017, pp. 1–6.

[159] H. Oh, G. S. May, and M. S. Bakir, "Analysis of signal propagation through TSVs within distilled water for liquid-cooled microsystems," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1176–1181, Mar. 2016.

[160] Y. Zhang and M. S. Bakir, "Independent interlayer microfluidic cooling for heterogeneous 3D IC applications," *Electron. Lett.*, vol. 49, no. 6, pp. 404–406, Mar. 2013.

[161] Z. Wan, H. Xiao, Y. Joshi, and S. Yalamanchili, "Co-design of multicore architectures and microfluidic cooling for 3D stacked ICs," in *Proc. 19th Int. Workshop Thermal Investigations ICs Syst. (THERMINIC)*, Sep. 2013, pp. 237–242.

[162] Z. Yang and A. Srivastava, "Co-placement for pin-fin based microfluidically cooled 3D ICs," *Thermal Manage.*, vol. 53, no. 9, pp. 1689–1699, 2015.

[163] B. Rakesh, K. Mahindra, M. S. V. Goud, N. A. Vignesh, T. Padma, and A. K. Panigrahy, "Facile approach to mitigate thermal issues in 3D IC integration using effective FIN orientation," *Mater. Today, Proc.*, vol. 33, pp. 3085–3088, 2020.

[164] S. Feng, Y. Yan, H. Li, L. Zhang, and S. Yang, "Thermal management of 3D chip with non-uniform hotspots by integrated gradient distribution annular-cavity micro-pin fins," *Appl. Thermal Eng.*, vol. 182, Jan. 2021, Art. no. 116132.

[165] Y. J. Kim, Y. K. Joshi, A. G. Fedorov, Y.-J. Lee, and S.-K. Lim, "Thermal characterization of interlayer microfluidic cooling of three-dimensional integrated circuits with nonuniform heat flux," *J. Heat Transf.*, vol. 132, no. 4, pp. 1–9, Apr. 2010.

[166] Y. Madhour, B. P. d'Entremont, J. B. Marcinichen, B. Michel, and J. R. Thome, "Modeling of two-phase evaporative heat transfer in three-dimensional multicavity high performance microprocessor chip stacks," *J. Electron. Packag.*, vol. 136, no. 2, pp. 1–10, Jun. 2014.

[167] A. Sridhar, Y. Madhour, D. Atienza, T. Brunschwiler, and J. Thome, "STEAM: A fast compact thermal model for two-phase cooling of integrated circuits," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2013, pp. 256–263.

[168] P. R. Parida *et al.*, "Modeling embedded two-phase liquid cooled high power 3D compatible electronic devices," in *Proc. 33rd Thermal Meas., Modeling Manage. Symp. (SEMI-THERM)*, 2017, pp. 130–138.

[169] D. Lorenzini and Y. Joshi, "Numerical modeling and experimental validation of two-phase microfluidic cooling in silicon devices for vertical integration of microelectronics," *Int. J. Heat Mass Transf.*, vol. 138, pp. 194–207, Aug. 2019.

[170] D. Lorenzini and Y. K. Joshi, "Computational fluid dynamics modeling of flow boiling in microchannels with nonuniform heat flux," *J. Heat Transf.*, vol. 140, no. 1, pp. 1–11, Jan. 2018.

[171] U. K. Alugoju, S. K. Dubey, and A. Javed, "3D transient heat transfer analysis and flow visualization study in diverging microchannel for instability mitigated two-phase flow: A numerical study," *Int. J. Heat Mass Transf.*, vol. 160, Oct. 2020, Art. no. 120212.

[172] D. D. Ma, G. D. Xia, L. X. Zong, Y. T. Jia, Y. X. Tang, and R. P. Zhi, "Experimental investigation of flow boiling heat transfer performance in zigzag microchannel heat sink for electronic cooling devices," *Int. J. Thermal Sci.*, vol. 145, Nov. 2019, Art. no. 106003.

[173] B. R. R. Bapu, S. Kayalvizhi, and S. Murugavalli, "Two phase cooling with nano-fluid for highly dense electronic systems-on-chip—A pilot study," *Microelectron. Rel.*, vol. 108, May 2020, Art. no. 113640.

[174] E. G. Colgan *et al.*, "High performance and subambient silicon microchannel cooling," *J. Heat Transf.*, vol. 129, no. 8, p. 1046, 2007.

[175] Y. Zhang, A. Dembla, Y. Joshi, and M. S. Bakir, "3D stacked microfluidic cooling for high-performance 3D ICs," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, May 2012, pp. 1644–1650.

[176] L.-M. Collin *et al.*, "Add-on microchannels for hotspot thermal management of microelectronic chips in compact applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 3, pp. 434–445, Mar. 2019.

[177] D. Kong *et al.*, "Single-phase thermal and hydraulic performance of embedded silicon micro-pin fin heat sinks using R245fa," *Int. J. Heat Mass Transf.*, vol. 141, pp. 145–155, Oct. 2019.

[178] C. R. Kharangate *et al.*, "Experimental investigation of embedded micropin-fins for single-phase heat transfer and pressure drop," *J. Electron. Packag.*, vol. 140, no. 2, Jun. 2018.

[179] A. Alqahtani, Z. Ren, J. Lee, and N. Bagherzadeh, "System-level analysis of 3D ICs with thermal TSVs," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 14, no. 3, pp. 1–16, Nov. 2018.

[180] F. Wang, Y. Li, N. Yu, and Y. Yang, "Effectiveness of thermal redistribution layer in cooling of 3D ICs," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. e2847, pp. 1–10, Nov. 2020.

[181] P. Franzon, J. Wilson, and M. Li, "Thermal isolation in 3D chip stacks using vacuum gaps and capacitive or inductive communications," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Nov. 2010, pp. 1–4.

[182] S. Hu *et al.*, "A thermal isolation technique using through-silicon vias for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1282–1287, Mar. 2013.

[183] A. Barua, M. S. Hossain, K. I. Masood, and S. Subrina, "Thermal management in 3-D integrated circuits with graphene heat spreaders," *Phys. Procedia*, vol. 25, pp. 311–316, Jan. 2012.

[184] S. K. Vendra and M. Chrzanowska-Jeske, "Thermal management in 3D IC designs for nano-CMOS technologies: Analysis on graphene- vs. graphite-based TIM," in *Proc. IEEE 13th Nanotechnol. Mater. Devices Conf. (NMDC)*, Oct. 2018, pp. 1–4.

[185] H.-C. Chien *et al.*, "Thermal evaluation and analyses of 3D IC integration SiP with TSVs for network system applications," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, no. 195, May 2012, pp. 1866–1873.

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[186] L. Hou, T. Ye, Q. Luo, J. Fu, and J. Wang, "A method to alleviate hot spot problem in 3D IC," *Microelectronic Eng.*, vol. 190, pp. 19–27, Apr. 2018.

[187] H. Oprins *et al.*, "Characterization of the thermal impact of cu-cu bonds achieved using TSVs on hot spot dissipation in 3D stacked ICs," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May 2011, pp. 861–868.

[188] Y. Chen, E. Kursun, D. Motschman, C. Johnson, and Y. Xie, "Through silicon via aware design planning for thermally efficient 3-D integrated circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 9, pp. 1335–1346, Sep. 2013.

[189] S. Singh, A. Kumar Panigrahi, O. Krishan Singh, and S. Govind Singh, "Analysis of graphene and CNT based finned TTSV and spreaders for thermal management in 3D IC," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Nov. 2016, pp. 1–4.

[190] M. M. Sabry Aly *et al.*, "The N3XT approach to energy-efficient abundant-data computing," *Proc. IEEE*, vol. 107, no. 1, pp. 19–48, Jan. 2019.

[191] N. M. Hossain, M. Hossain, A. H. B. Yousuf, and M. H. Chowdhury, "Thermal aware graphene based through silicon via design for 3D IC," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Oct. 2013, pp. 1–4.

[192] K. Furumi, M. Imai, and A. Kurokawa, "Cooling architectures using thermal sidewalls, interchip plates, and bottom plate for 3D ICs," in *Proc. 18th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2017, pp. 283–288.

[193] J. H. Lau *et al.*, "Through-silicon hole interposers for 3-D IC integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 9, pp. 1407–1419, Sep. 2014.

[194] B. Shi, A. Srivastava, and A. Bar-Cohen, "Co-design of microfluidic heat sink and thermal through-silicon-vias for cooling of three-dimensional integrated circuit," *IET Circuits, Devices Syst.*, vol. 7, no. 5, pp. 223–231, Sep. 2013.

[195] S. K. Roy, S. Mandal, C. Giri, and H. Rahman, "A thermal estimation model for 3D IC using liquid cooled microchannels and thermal TSVs," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, Oct. 2015, pp. 122–127.

[196] K.-J. Wang, H.-C. Sun, C.-L. Li, G.-D. Wang, and H.-W. Zhu, "Thermal management of the hotspots in 3-D integrated circuits," *Thermal Sci.*, vol. 22, no. 4, pp. 1685–1690, 2018.

[197] M. Park, S. Kim, and S. E. Kim, "Evaluation of Si liquid cooling structure with microchannel and TSV for 3D application," *Microsyst. Technol.*, vol. 23, no. 7, pp. 2609–2614, Jul. 2017.

[198] M. S. Shamim, R. S. Narde, J.-L. Gonzalez-Hernandez, A. Ganguly, J. Venkatarman, and S. G. Kandlikar, "Evaluation of wireless network-on-chip architectures with microchannel-based cooling in 3D multicore chips," *Sustain. Comput., Informat. Syst.*, vol. 21, pp. 165–178, Mar. 2019.

[199] T. Brunschwiler, A. Sridhar, C. Lee Ong, and G. Schlottig, "Benchmarking study on the thermal management landscape for three-dimensional integrated circuits: From back-side to volumetric heat removal," *J. Electron. Packag.*, vol. 138, no. 1, pp. 010911:1–010911:10, Mar. 2016.

[200] H. Oh, Y. Zhang, L. Zheng, G. S. May, and M. S. Bakir, "Fabrication and characterization of electrical interconnects and microfluidic cooling for 3D ICS with silicon interposer," *Heat Transf. Eng.*, vol. 37, no. 11, pp. 903–911, Jul. 2016.

[201] L. Zheng, Y. Zhang, X. Zhang, and M. S. Bakir, "Silicon interposer with embedded microfluidic cooling for high-performance computing systems," in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 828–832.

[202] Y. Zhang, T. E. Sarvey, and M. S. Bakir, "Thermal challenges for heterogeneous 3D ICs and opportunities for air gap thermal isolation," in *Proc. Int. 3D Syst. Integr. Conf. (3DIC)*, vol. 2, Dec. 2014, pp. 1–5.

[203] Y. Zhang, Y. Zhang, T. Sarvey, C. Zhang, M. Zia, and M. Bakir, "Thermal isolation using air gap and mechanically flexible interconnects for heterogeneous 3-D ICs," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 1, pp. 31–39, Jan. 2016.

[204] D. Lorenzini *et al.*, "Embedded single phase microfluidic thermal management for non-uniform heating and hotspots using microgaps with variable pin fin clustering," *Int. J. Heat Mass Transf.*, vol. 103, pp. 1359–1370, Dec. 2016.

[205] Z. Yan, M. Jin, Z. Li, G. Zhou, and L. Shui, "Droplet-based microfluidic thermal management methods for high performance electronic devices," *Micromachines*, vol. 10, no. 2, p. 89, Jan. 2019.

[206] Y. S. Lee, K. M. Kim, J. H. Lee, Y.-H. Gong, S. W. Kim, and S. W. Chung, "Monolithic 3D stacked multiply-accumulate units," *Integration*, vol. 76, pp. 183–189, Jan. 2021.

[207] J. Jiang, K. Parto, W. Cao, and K. Banerjee, "Ultimate monolithic-3D integration with 2D materials: Rationale, prospects, and challenges," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 878–887, 2019.

[208] S. Panth, K. Samadi, Y. Du, and S. K. Lim, "Placement-driven partitioning for congestion mitigation in monolithic 3D IC designs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 34, no. 4, pp. 540–553, Apr. 2015.

[209] W. C.-Y. Ma, Y.-J. Huang, P.-J. Chen, J.-W. Jhu, Y.-S. Chang, and T.-H. Chang, "Impacts of vertically stacked monolithic 3D-IC process on characteristics of underlying thin-film transistor," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 724–730, 2020.

[210] S. Rangachar Srinivasa *et al.*, "ROBIN: Monolithic-3D SRAM for enhanced robustness with in-memory computation support," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 7, pp. 2533–2545, Jul. 2019.

[211] S. Tang *et al.*, "Fabrication of low cost and low temperature polysilicon nanowire sensor arrays for monolithic three-dimensional integrated circuits applications," *Nanomaterials*, vol. 10, no. 12, p. 2488, Dec. 2020.

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